LEVEL II

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DOPPLER ACOUSTIC VORTEX SENSING SYSTEM

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FINAL REPORT

Prepared for

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION
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Washington DC 20591

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16. Abstract

This is the final report on the Doppler Acoustic Vortex Sensing System (DAVSS) program carried out by Avco Corporation's Systems Division for the U.S. Department of Transportation, Transportation Systems Center.

This program was carried out under Contract DOT-TSC-710, dated 12 November 1973. The objective of the program was the design of an engineered DAVSS capable of real-time detection, tracking, recording, and graphic display of aircraft trailing vortices. Problems related to such vortices are currently under intensive study by the U.S. Department of Transportation for the Federal Aviation Administration.

This report presents hardware and software design aspects of the system. The design of the acoustic antennas and transducers is described. System control, computer hardware and software, and system/subsystem interfaces are discussed.

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PREFACE

The problems related to aircraft trailing vortices are currently under intensive study for the Federal Aviation Administration (FAA) by the U.S. Department of Transportation (DOT). The Transportation Systems Center (TSC) of the DOT initiated and is carrying out several programs in this area, including programs to develop acoustic systems for detecting, tracking, and measuring the strength of aircraft wake vortices. The system described in this report was designed, built, and tested by Avco Corporation's Systems Division (Avco/SD) for DOT/TSC under Contract DOT-TSC-710, dated 12 November 1973. It is an engineered, flexible acoustic radar capable of operating in several different modes to test Doppler acoustic radar techniques that use turbulent scattering for wake vortex detection and tracking.

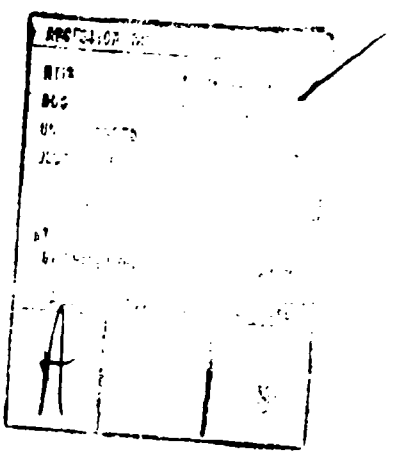
The Avco-engineered system is designed to permit operation of either one (of two) 4-element arrays deployed along an appropriate baseline in the following-listed alternative modes:

1. Continuous wave (CW) bistatic forward scatter
2. Pulsed bistatic forward scatter
3. Pulsed backscatter, either
    a. Bistatic, or
    b. Monostatic

to provide real-time detection, tracking, recording, and graphic displaying of vortex locations.

This final report describes the design and implementation of the engineered system. It covers both the hardware and software designs as well as some description of system operation and early test results.

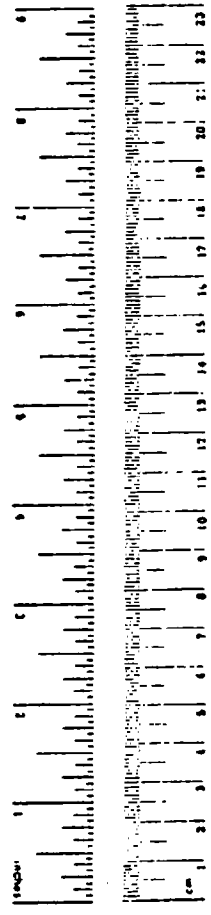
The work performed under this contract was significantly enhanced by the close cooperation and contributions of Ralph Kodis, David Burnham, and Thomas Sullivan, all of DOT/TSC.



METRIC CONVERSION FACTORS

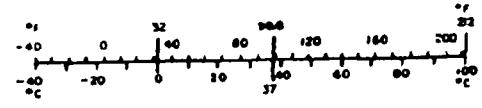
Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
	inches	2.5	centimeters	cm
	feet	30	centimeters	cm
	yards	0.9	meters	m
	miles	1.6	kilometers	km
		AREA		
	square inches	6.5	square centimeters	cm^2
	square feet	0.09	square meters	m^2
	square yards	0.8	square meters	m^2
	square miles	2.6	square kilometers	km^2
	acres	0.4	hectares	ha
		MASS (weight)		
	ounces	28	grams	g
	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
		VOLUME		
	teaspoons	5	milliliters	ml
	tablespoons	15	milliliters	ml
	fluid ounces	30	milliliters	ml
	cups	0.24	liters	l
	pints	0.47	liters	l
	quarts	0.95	liters	l
	gallons	3.8	liters	l
	cubic feet	0.03	cubic meters	m^3
	cubic yards	0.76	cubic meters	m^3
		TEMPERATURE (exact)		
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C



Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
		AREA		
cm^2	square centimeters	0.16	square inches	in^2
m^2	square meters	1.2	square yards	yd^2
km^2	square kilometers	0.4	square miles	mi^2
ha	hectares (10,000 m^2)	2.5	acres	
		MASS (weight)		
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
		VOLUME		
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m^3	cubic meters	35	cubic feet	ft^3
m^3	cubic meters	1.3	cubic yards	yd^3
		TEMPERATURE (exact)		
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F



CONTENTS

CONTENTS (Cont'd.)

CONTENTS (Concl'd.)

ILLUSTRATIONS

ILLUSTRATIONS (Cont'd.)

ILLUSTRATIONS (Cont'd.)

ILLUSTRATIONS (Concl'd.)

TABLES

ABBREVIATIONS AND SYMBOLS

A/D	Analog-to-digital
ASCII	American Standard Code for Information Interchange
A/SD	Avco Corporation, Systems Division
AVMOTS	Avco Modular Test System
AWG	American wire gauge
BCD	Binary coded decimal
BOT	Beginning of tape
CRT	Cathode ray tube
CSR	Command status register
CW	Continuous wave
DAS	Data acquisition subsystem
DARS	Doppler acoustic radar subsystem
DAVSS	Doppler acoustic vortex sensing system
dB	Decibel
D/A	Digital-to-analog
DDS	Data display subsystem
DEC	Digital Equipment Corporation
DMA	Direct memory address
DOT	Department of Transportation (U.S.)
DOT/TSC	Department of Transportation, Transportation Systems Center (U.S.)
DSS	Data storage subsystem
EMI	Electromagnetic interference

ABBREVIATIONS AND SYMBOLS (Cont'd)

EOR	End of run
EOT	End of tape
FAA	Federal Aviation Administration (U.S.)
Fn	Frequency n
F/D	Focal length-to-diameter ratio
GFE	Government-furnished equipment
hit	Acoustic data pulse
Hz	Hertz (one cycle per second)
ID	Identity (or identification)
ips	Inch (es) per second
IRIG	Inter-Range Instrumentation Group
I/O	Input/output
J-box	Junction box
kHz	Hz x 1000
k	1000
M	1,000,000
MDAC	Multiplying digital-to-analog converter
MHz	Hz x 1,000,000
msec	Millisecond
n	A sequentially assigned integer, e.g., R28 is the 28th resistor
NAFEC	National Aviation Facilities Experimental Center (U.S.)

ABBREVIATIONS AND SYMBOLS (Concl'd)

NRZ	Non-return to zero
Op amp	Operational amplifier
PVC	Polyvinyl chloride
Qn	Transistor n
RCB	Radar controller board
Rn	Resistor n
RTV	Room temperature vulcanizing
SOR	Start of run
Sync	Synchronization
TSC	Transportation Systems Center (U.S.)
TTL	Transistor-transistor logic
Y, and Z	Acoustic radar arrays Y and Z
Zn	Integrated circuit n
λ	Wavelength at the frequency of interest.

1. INTRODUCTION

Trailing vortices from heavy jet aircraft represent a currently undefined hazard, particularly during landing and takeoff operations. Considerations of safety and the need to optimize airport operations make it essential to acquire positive information about the presence and locations of vortices generated by heavy aircraft. The feasibility of using Doppler acoustic radars sensitive to the turbulent scattering caused by wake vortices to detect and track their progress has been demonstrated by Department of Transportation's Transportation Systems Center (DOT/TSC) tests at John F. Kennedy International Airport, National Oceanic and Atmospheric Administration (NOAA) tests near Denver, Colorado, and Federal Aviation Administration (FAA) sponsored tests at the National Aviation Facilities Experimental Center (NAFEC), Atlantic City, New Jersey. The hardware used during these tests were either laboratory models or equipment designed to investigate only one aspect of the wake vortex detection and tracking situation. The equipment was not engineered for long-term installation in the field, and incapable of automatic real-time data processing and display.

This report describes a Doppler acoustic vortex sensing system (DAVSS) development program carried out by Avco Systems Division (Avco/SD) for DOT/TSC under Contract DOT-TSC-710. The goal of this program was to develop, build, and test an engineered Doppler acoustic wake vortex sensing system consisting of acoustic sensors and associated electronics capable of operating in both monostatic and bistatic siting configurations to acquire and process the sensed data and to display this data visually in real time.

This final report consists of four sections and four appendixes, as follows:

Section 2 describes the over-all system

Section 3 discusses the design of the individual subsystems and sub elements

Section 4 describes system operation

Appendix A presents the Drawing List

Appendix B contains the Parts List

Appendix C gives the early results of system field tests at Logan International Airport, Boston, MA, and

Appendix D reports on inventions.

2. SYSTEM DESCRIPTION

This section describes the Doppler acoustic vortex sensing system (DAVSS) from a systems viewpoint.

2.1 GENERAL

The DAVSS consists of two 4-element acoustic radar antenna arrays and all the hardware, software, and interface items necessary for real-time acquisition, reduction, readout, and display of vortex position data. Analog and digital data is stored on magnetic tape for subsequent off-line reduction and evaluation. The system contains a minicomputer which not only performs the required DAVSS functions but also can interface with other external computers or control systems. The system may be considered to consist of the following listed basic subsystems:

Doppler acoustic radar subsystem (DARS)

Data acquisition subsystem (DAS)

Data display subsystem (DDS)

Data storage subsystem (DSS)

Software subsystem.

Figure 2-1 is a pictorial overview of the DAVSS. Brief functional descriptions of each of these subsystems follow.

2.1.1 Doppler Acoustic Radar Subsystem

The Doppler acoustic radar subsystem consists of two arrays, each containing two transmitting antenna assemblies and two receiving antenna assemblies. Each transmitting antenna assembly consists of: (a) a dual-channel Phase Linear Amplifier and shelter; (b) two Altec Lansing 290 E acoustic drivers; (c) a feed, combiner, and horn subassembly; (d) a reflector, shroud, and mounting structure; and (e) interconnecting cables.

Each receiving antenna assembly consists of: (1) a 12-channel horn-microphone-receiver subassembly; (2) a parabolic dish, shroud, and mounting structure; and (3) interconnecting cables. The array elements are designed to allow two independent arrays to be deployed, each with baseline length up to 1000 ft.

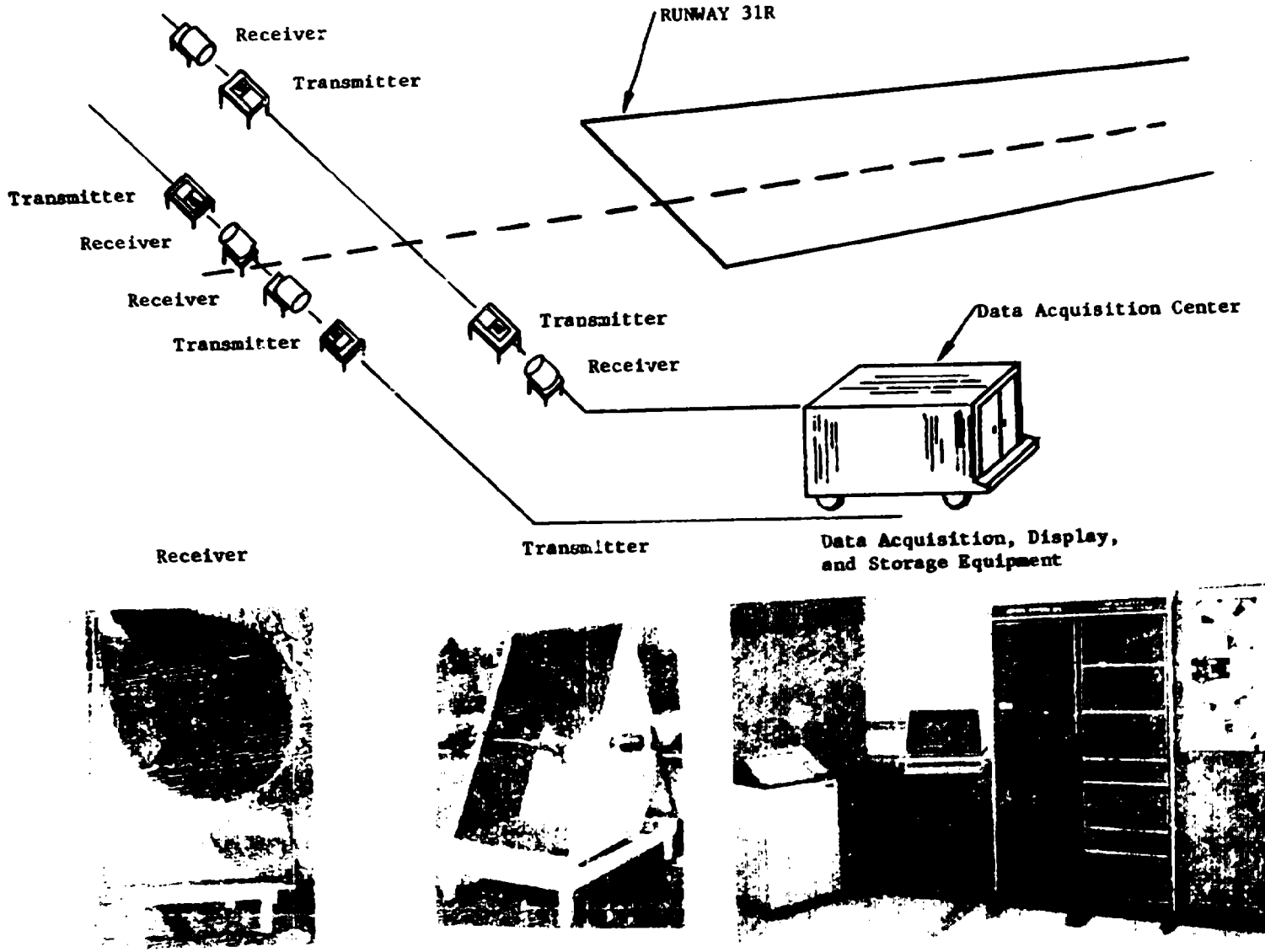


FIGURE 2-1. PICTORIAL VIEW, DOPPLER ACOUSTIC VORTEX SENSING SYSTEM

2.1.2 Data Acquisition Subsystem

The data acquisition subsystem contains the minicomputer and all of the electronic equipment needed to: (1) select an array configuration; (2) generate modulation wave forms; (3) receive, discriminate, and detect transmitted signals; (4) extract angle and range (in pulsed mode) information; (5) determine vortex position information; and (6) control data storage and display subsystems. The minicomputer performs these functions automatically in response to computer programs generated off-line and entered into the computer memory via a digital magnetic tape recorder interface. The system is also controlled by appropriate keyboard inputs. The minicomputer provides 16,000 (16k) words of memory. A data link to a central controller permits remote control of the system.

2.1.3 Data Display Subsystem

The data display subsystem consists of a cathode ray tube (CRT) display, and a hard-copy display to allow printout of selected data, computer calculations, and graphic data. The displays are used to present vortex position data from an array. Either display operates in a real time, two-dimensional mode -- that is, it displays, for example, altitude and horizontal displacement with respect to a runway centerline as a function of time. Alternatively, the CRT can be used to display vortex track motion in the vertical plane of the sensor.

2.1.4 Data Storage Subsystem

The data storage subsystem consists of two magnetic tape recorders, one analog and the other digital. The former is a 28-track unit, the latter a 9-track recorder.

The analog recorder provides direct recording of pre-amplified, equalized, and bandpassed receiver signals (acoustic returns), array time-reference signals, run initiation and run identification data, configuration definition data, and voice commentary. During playback, the directly recorded signal may be processed and displayed in the same manner as data is processed and displayed during operations in real time.

The primary function of the digital tape recorder is to store time-delay and vortex position data during periods of unattended operation. Its secondary function is to serve as an input/output device to facilitate loading and readout of computer programs.

2.1.5 Software Subsystem

The software subsystem consists of all computer programs required to: operate the DAVSS, produce the graphic displays, and record vortex track data.

2.2 OVER-ALL SYSTEM DESCRIPTION

This section presents the over-all design of the DAVSS. The various subsystems are described in detail in Section 3.0.

The DAVSS hardware system is shown in block diagram form in Figure 2-2. As noted above, it consists of the following-listed subsystems: Doppler acoustic radar subsystem, data acquisition subsystem, data display subsystem, and data storage subsystem.

The Doppler acoustic radar subsystem consists of eight acoustic antennas -- four transmitting and four receiving antennas. These are used in two arrays, each consisting of two transmitters and two receivers. The transmitting antennas are all alike as are the receiving antennas. The transmitting antennas are designed to deliver a uniform fan beam of acoustic energy, whose width is 5° in the azimuthal plane and selectable as 37°, 45°, or 60° in the elevation plane. The beam center is settable in the elevation plane from 15° to 90° above the horizon. Each transmitting antenna consists of a parabolic cylinder reflector activated by center-mounted rectangular aperature feed horns that are driven by two Altec Lansing 290 E loudspeakers capable of handling 100 watts input each. Their outputs are transmitted from outside the secondary aperture by acoustic transmission lines and combined using Altec 30170 combiners with two Altec 30546 -45° elbows. To reduce the sidelobe response of the transmitting antenna, a 4-foot long sidelobe suppressing shroud which is flared 30° outward in the vertical plane is attached to the reflector. To avoid line loss and distortion over the long lines between the data acquisition subsystem and the antennas, the transmitter signal is delivered at low power and amplified at the transmitting antenna by a Phase Linear 400 dual-channel amplifier.

The receiving antennas are designed to produce twelve $3^{\circ} \times 3^{\circ}$ pencil beams, each separated by 3° in the elevation plane. In addition, this comb of twelve beams is settable in the elevation plane so that the center beam may be positioned from 15° to 90° above the horizon. Thus, horizon-to-horizon coverage is available with both the transmitting and receiving antennas. The resultant comb of twelve beams is formed by placing a linear array of twelve mini horn-microphone-

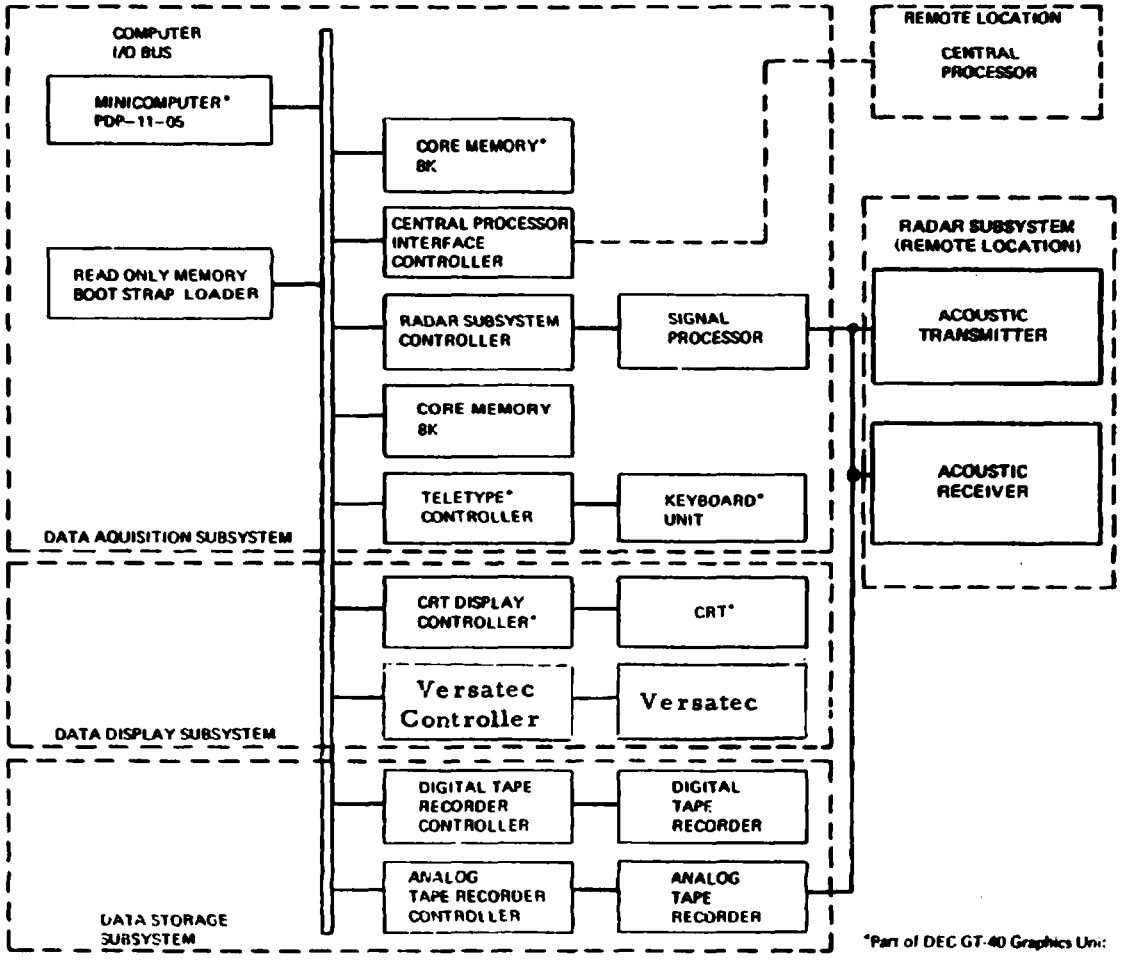


FIGURE 2-2. DOPPLER ACOUSTIC VORTEX SENSING SYSTEM-BLOCK DIAGRAM

receiver channels across the focal plane of a 6-foot parabolic reflecting dish whose focal length is 37 inches. The parabolic dish is also shrouded by an 8-foot long, 6-foot inside diameter (ID) cylindrical sidelobe suppressor lined with 1-inch thick Coustex absorber. The nominal aperture of the 3-inch long primary horns is 2 inches and the set of 12 are spaced 2" on center. The microphones are TELectret™ (Model 5336C) miniature condenser microphones with integral preamplifiers. A twelve-channel band pass and preamplifier stage is provided in the horn-microphone-receiver assembly to reduce susceptibility to noise and interference pickup over the long lines back to the DAS.

The data acquisition subsystem contains all of the elements needed to control system operation (upon receipt of external data either from a central processor or local keyboard), solve for vortex locations, and feed data to the display or storage subsystems. Data acquisition subsystem elements include a PDP-11/05 minicomputer, with extended arithmetic capability; a bootstrap loader; a core memory (additional to that provided in the minicomputer); a radar subsystem controller; a keyboard unit and associated controller; and an analog signal processor.

The data display subsystem consists of a Digital Equipment Corporation (DEC) GT-40 graphics unit that includes a CRT for visual presentation of data. Software is provided to allow use of a Versatec Model 1109A hard-copy display device for presentation of data, including graphics. The data storage subsystem consists of two magnetic tape recorders and their associated controllers. One tape recorder, used for analog data, is a Bell and Howell VR3700B 28-track recorder with provision for voice recording/playback on an edge track. The other is a DEC TU-10, 9-track recorder used for digital data.

The combined data acquisition, display, and storage subsystems are housed as shown in Figure 2-3.

FIGURE 2-3. DATA ACQUISITION DISPLAY AND STORAGE HARDWARE

3. SUBSYSTEM DESIGN

This portion of the final report includes detailed discussions and descriptions of the design of each subsystem of the DAVSS.

3.1 DOPPLER ACOUSTIC RADAR SUBSYSTEM

The Doppler acoustic radar subsystem consists of four identical transmitting antenna assemblies and four receiving antenna assemblies, each complete with acoustic transducers and associated electronics. It also includes the required interconnecting signal and power cabling. (Primary power -- 117V, 60Hz, AC is assumed to be provided at the individual antenna sites.) The acoustic antenna elements and the signal and power distribution layouts are described in Paragraphs 3.1.1, 3.1.2, and 3.1.3.

3.1.1 Transmitting Antenna Assemblies

The transmitting antenna assembly consists of the following components:

1. Reflector, feed horn, shroud, and support structure.
2. Horn - driver subassembly, composed of:

   A selection of 3 rectangular excitation horns

   3.7" x 4.35" x 8" for 60° x 5°

   5.0" x 4.35" x 8" for 45° x 5°

   6.0" x 4.35" x 8" for 37° x 5°

   Drivers - 2 Altec Lansing 290E's, 100-watt input

   Pipes and Flanges - 1.4" ID

   Combiner - Altec 30170 with two 30546 45° elbows.
3. Acoustic Signal Amplifier and Housing

   Phase Linear - 400

   Louvered Environmental Enclosure.

These major items are described below.

3.1.1.1 Reflector, Feed Horn, Shroud, and Support Structure

The following paragraphs describe the acoustic design and the mechanical design and construction of the reflector, the feed horn, the shroud and the support structure.

Acoustic Design

The reflector design selected for the DAVSS was chosen on the basis of its ability to: (1) satisfy the acoustic radiation pattern requirements specified in Table 3-1, (2) meet the field equipment environmental and physical design requirements listed in Table 3-2, and (3) have the greatest commonality with the already proven pulsed acoustic vortex sensing system (PAVSS) design. Initial measurements made with the 36-inch by 52-inch parabolic reflector used in the PAVSS gave assurance that the design requirements for frequency and beamwidth were met using a center-mounted rectangular feed as the primary aperture. Three rectangular feed horns were cut, measured, and sent out for fabrication in fiberglass. Their sizes are:

$37^{\circ} \times 5^{\circ}$	6.0" x 4.35" x 8"
$45^{\circ} \times 5^{\circ}$	5.0" x 4.35" x 8"
$60^{\circ} \times 5^{\circ}$	3.7" x 4.35" x 8".

In order to reduce the sidelobes in both the elevation and azimuthal plane, a rectangular aperture and shroud was constructed on the parabolic cylinder reflector. The inner surface was lined with thicknesses of Coustex absorber material as follows: 1-inch thick along the vertical walls (affecting the azimuthal sidelobes) and 3-inches thick on the horizontal walls (affecting the elevation sidelobes). In addition, the horizontal walls were flared at 30° to accommodate the 60° elevation beamwidth. The resulting structure is shown in Figure 3-1. Figures 3-2 through 3-5 show the resulting beam patterns at 3, 4, and 5 kHz in the elevation plane and for 4 kHz in the azimuthal plane for the 60° horn. The results are also tabulated in Table 3-3.

TABLE 3-1

TRANSMITTING ANTENNA REQUIREMENTS

Frequency Range	3 to 5 kHz
Beamwidth (Fan) # at 4 kHz	
Elevation, ϕ, selectable	37°, 45°, 60°
Azimuth, θ	5°
Sidelobes at 4 kHz	
$\phi \geqq 45^\circ$	-30 db
$\theta \geqq 20^\circ$	-20 db
Transmit Power	200 watts electrical
	50 watts, acoustic
Elevation of beam	25° - 90° settable
Elevation coverage	$\pm$17 from beam center.

TABLE 3-2

SUMMARY OF ENVIRONMENTAL REQUIREMENTS

FOR FIELD EQUIPMENT

Environmental Condition	Subsystem Condition	
	Operating	Non-Operating
Temperature		
High (^{o}F)	125	140
Low (^{o}F)	-40	-65
Relative Humidity		
% (Condensing)	0 - 100	
Temperature (^{o}F)	75 to 85	
Precipitation		
Rain (in./hr.)	0.3	1.0
Snow Load (lb/ft^{2})	20	
Wind		
Steady (mph)	35	75

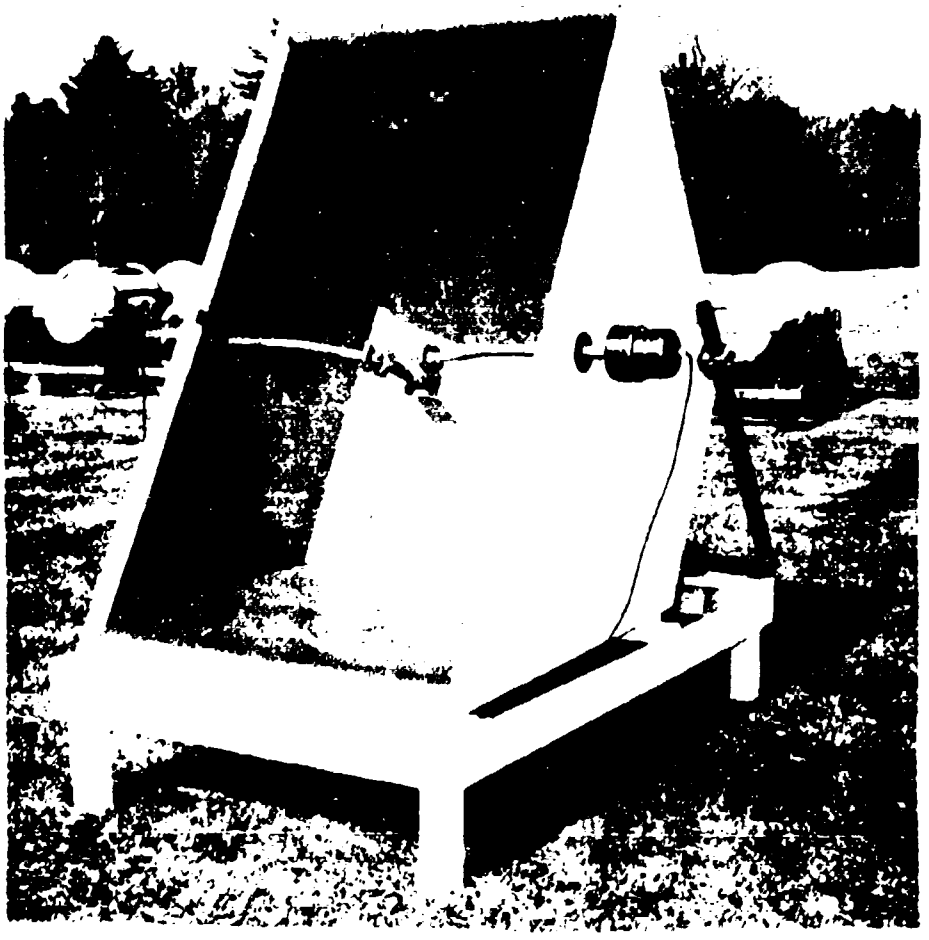
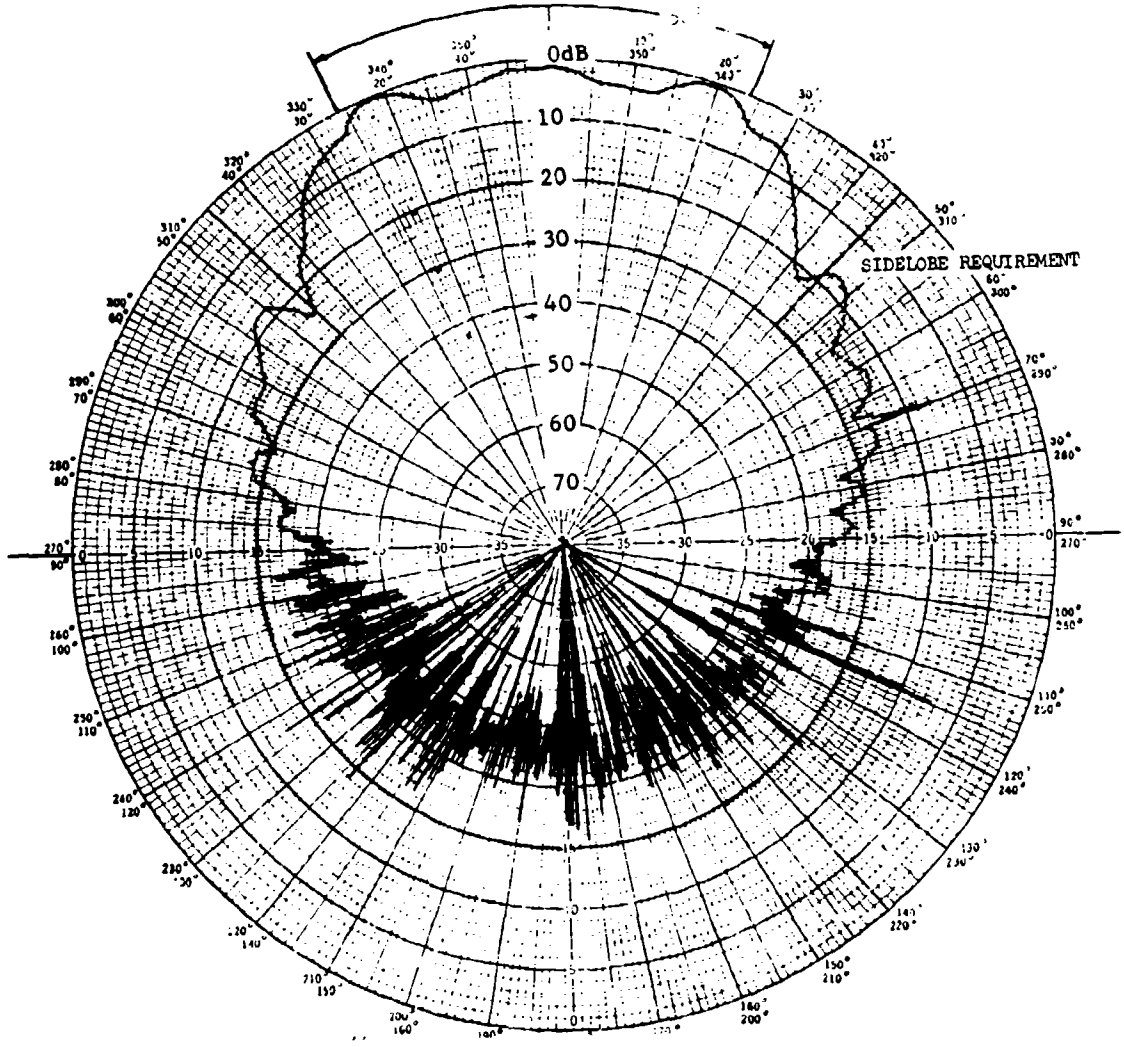


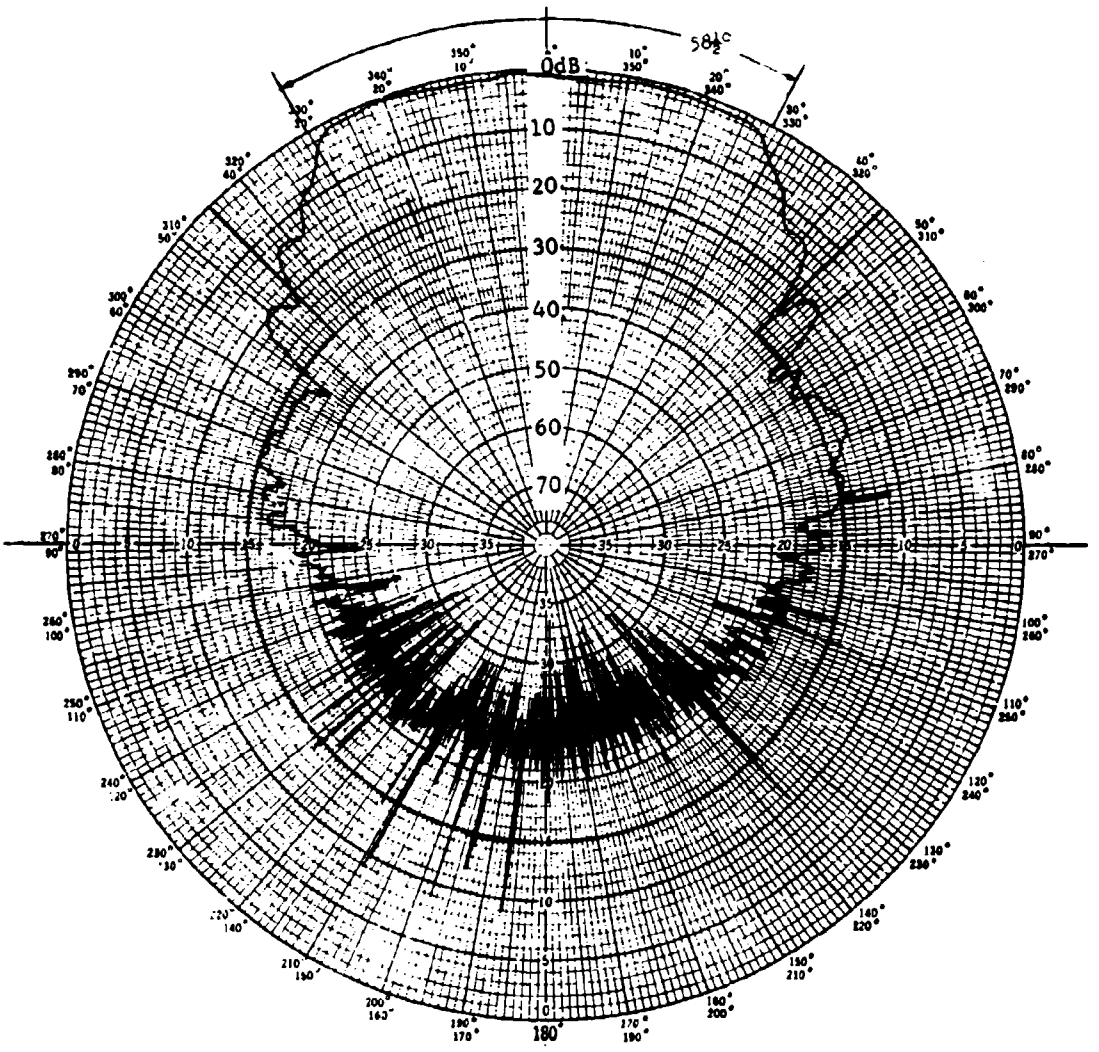
FIGURE 3-1. TRANSMITTING ANTENNA ASSEMBLY



3.7" x 4.35" x 8" HORN

60° NOMINAL PATTERN

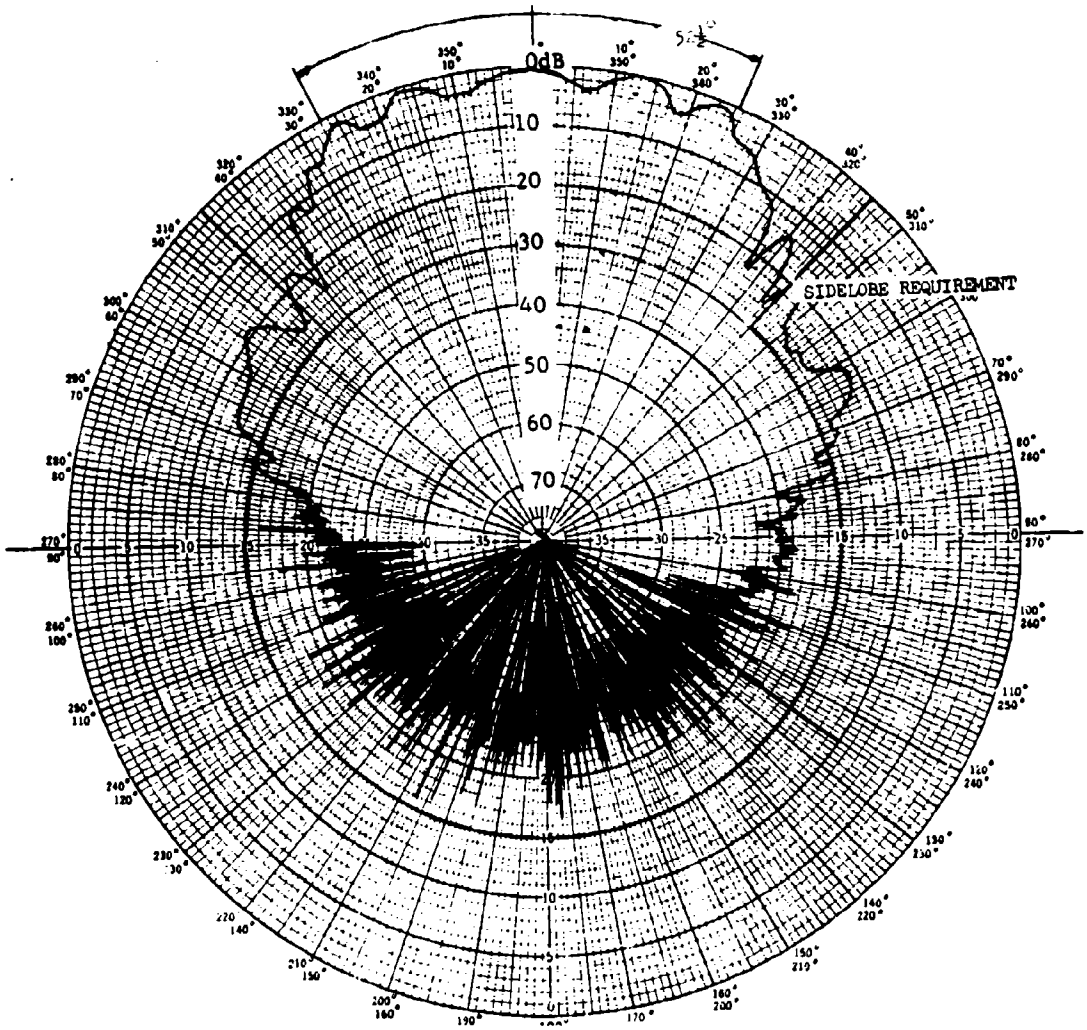
FIGURE 3-2. TRANSMITTING ANTENNA ELEVATION PLANE PATTERN, 3 kHz



3.7" x 4.35" x 8" HORN

60° NOMINAL PATTERN

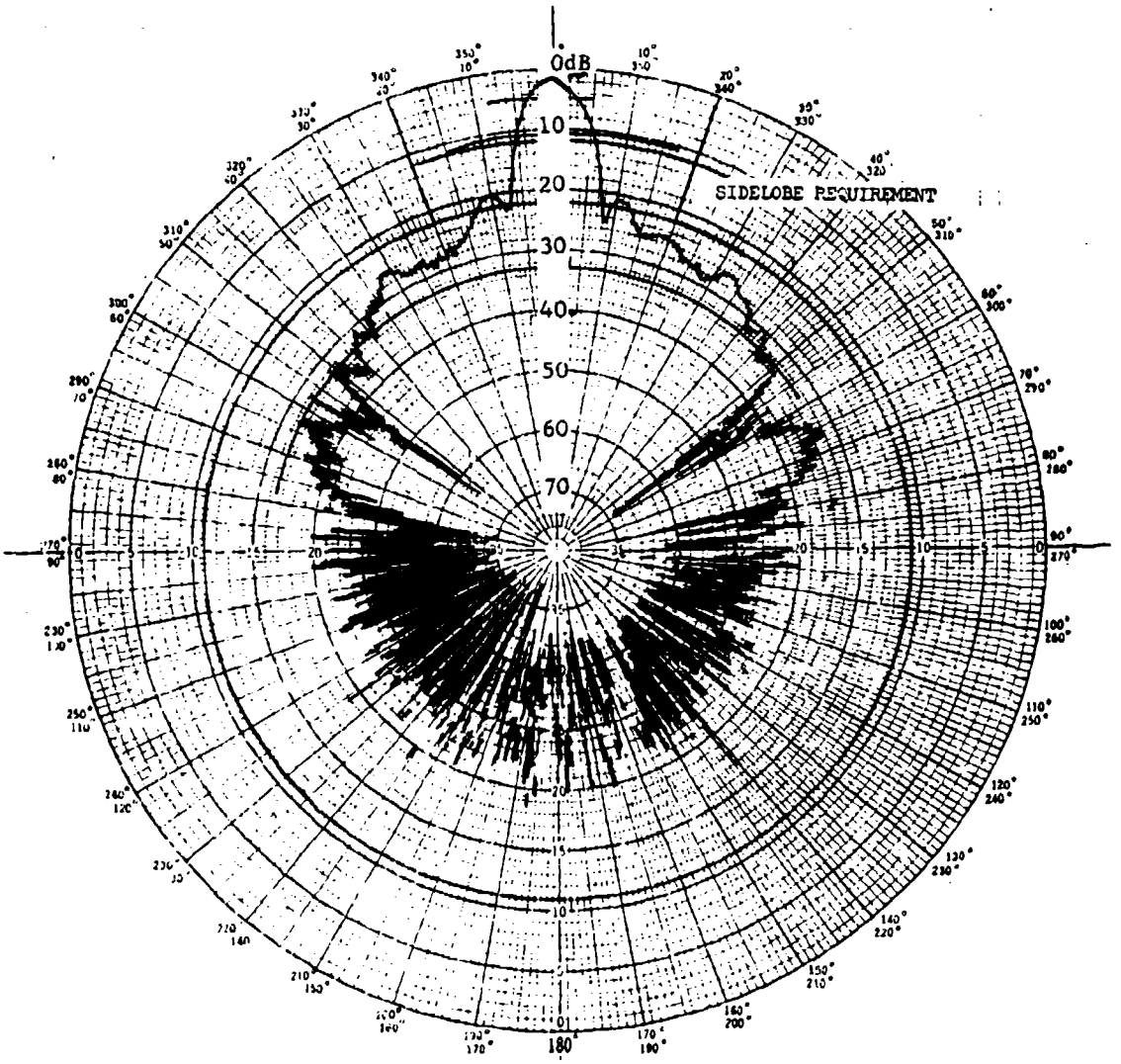
FIGURE 3-3. TRANSMITTING ANTENNA ELEVATION PLANE PATTERN, 4 kHz



3.7" x 4.35" x 8" HORN

60° NOMINAL PATTERN

FIGURE 3-4. TRANSMITTING ANTENNA ELEVATION PLANE PATTERN, 5 kHz



3.7" x 4.35" x 8" HORN

60° NOMINAL PATTERN

FIGURE 3-5. TRANSMITTING ANTENNA AZIMUTH PLANE PATTERN, 4 kHz

TABLE 3-3

TRANSMITTING ANTENNA MEASUREMENTS

• ELEVATION PLANE				
FREQ. KHZ	BEAMWIDTH		SIDELOBES	
	REQ'D	MEAS'D	REQ'D	MEAS'D
3.0	-	50°		-30 DB FOR 77% -40 DB FOR 66%
4.0	60°	58 1/2°	-30 DB @ ±45°	-30 DB FOR 86% -40 DB FOR 61%
5.0	-	52 1/2°		-30 DB FOR 80% -40 DB FOR 70%
• AZIMUTH PLANE				
FREQ. KHZ	BEAMWIDTH		SIDELOBES	
	REQ'D	MEAS'D	REQ'D	MEAS'D
3.0	-	7°	-	-20 DB FOR 100% -30 DB FOR 95%
4.0	5°	6°	-20 DB @ ±20°	-20 DB FOR 100% -30 DB FOR 83%
5.00	-	5 1/2°		-20 DB FOR 100% -30 DB FOR 85%

Mechanical Design - Reflector and Shroud

The reflector and shroud shown in Figure 3-1 consists of a cylindrical parabolic surface formed of Masonite which in integrally bonded to a braced marine-grade plywood box frame with extensions which form a rectangular trapezoidal shroud. The reflector is 36 inches high, has a chord of 52 inches and a focal length of 20 inches. The shroud has four sides, two of which are in the elevation plane and two in the azimuthal plane. The two sides in the elevation plane are isosceles trapezoidal sheets of plywood, 1/2-inch thick with a base of 7.58', a semi-base of 3.04' and an altitude of 3.90'. The elevation plane inside surfaces are lined with 1-inch thickness of Coustex acoustical absorbing material. The two sides in the azimuthal plane are 3.48' x 4.50' rectangular sheets of plywood. They are lined with three thicknesses of the 1-inch thick Coustex absorbing material. The corners are joined using 1.25" x 1.25" wood to which the plywood is bonded. All edges and corner joints are finished on the outside by 1.5" x 1.5" x 0.25" thick PVC angle stock.

Holes for draining rainwater are drilled in the bottom azimuthal plane sheet. Holes are drilled in the two elevation plane sheets for insertion of the horn-driver subassembly. The drivers are mounted outside the shroud on either side of the elevation plane portions of the shroud, and the acoustic energy is transmitted through the pipes to the combiner and horn. (See Figure 3-1.)

Mounting Structure

The mounting structure is integral to the transmitting antenna assembly. It consists of a wood frame with four 4" x 4" legs and 2" x 6" side rails. The top bearing surfaces are 2" x 8" boards on which the hinges are mounted. Figure 3-6 shows a rear view of the transmitting antenna assembly at low elevation. The reflector and shroud are hinged with two 6-inch T hinges so that the beam boresight may rotate from 30° above the horizon (as shown) to 90°. The reflector and shroud assembly is supported in position by means of PVC hardware swivel mounted at the rear of the stand and used to support each side of the shroud.

FIGURE 3-6. TRANSMITTING ANTENNA REAR VIEW

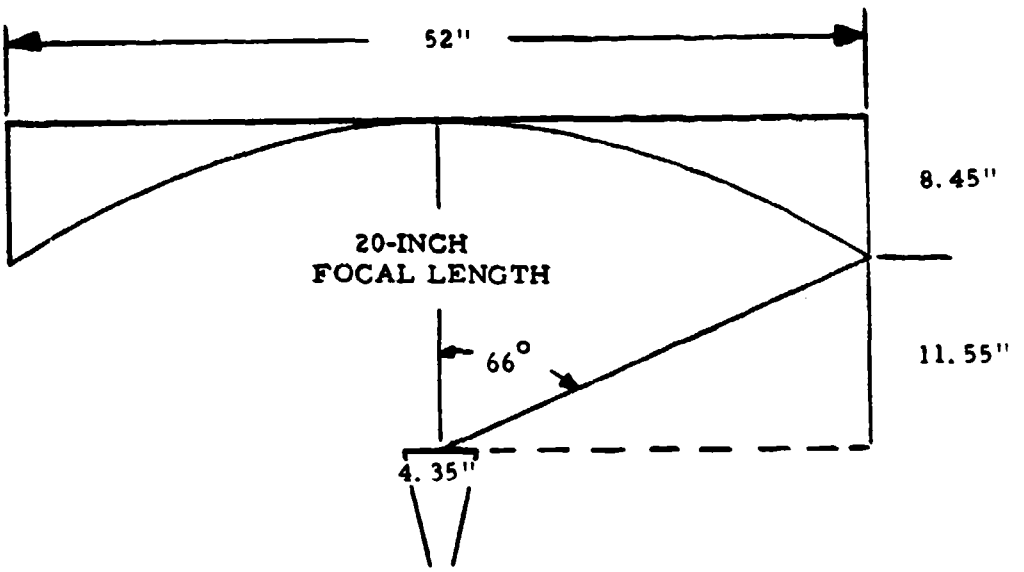
Two-inch diameter PVC pipe and elbows are fashioned into a "U". The base of the PVC "U" is supported in PVC blocks so that the "U" may rotate in elevation plane, as shown in Figure 3-6. T connectors and swivels are attached to the side of the shroud and bored out so that the PVC pipe can slide through as the reflector and shroud are rotated about its hinges through 30° - 90°. Positioning is accomplished by placing clamps above and below the slide mounting swivel around the PVC pipe. One clamp above on one side and below on the other. Dacron tie-down rope is attached at the upper apex of the shroud on each side and secured to four screwtype anchors.

3.1.1.2 Horn-Driver Subassembly

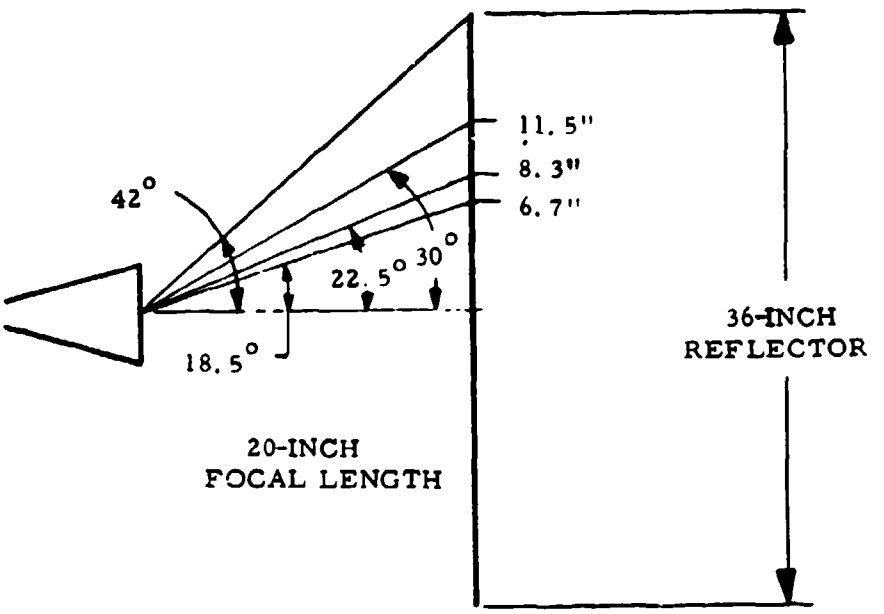
The goal of the driver-combiner-horn assembly development was to make it possible to deliver 50 acoustical watts from the primary aperture. The design approach taken was to select the most efficient drivers so that the fewest number of drivers could be combined to provide the desired acoustical output power. After extensive testing, it was determined that two Altec Lansing Model 290E drivers could be coupled, using off-the-shelf Altec combiners and elbows, to provide the nominal output power required.

Horns

The desired transmitting antenna pattern is fan-shaped, with beam dimensions of 5° (nominal) in the azimuthal plane and selectable at 37°, 45°, or 60° in the elevation plane. The reflector has a parabolic cylinder shape (parabolic in the azimuthal plane). The energy emanating from a horn placed at the focus will converge into the desired 5° azimuthal beam if the secondary reflector aperture is illuminated with a tapered pattern provided by the primary aperture dimension. Illumination of a 52" chord of a 20" focal length parabola requires a 4.35" primary aperture. In the elevation plane, the reflector is linear thus, the primary aperture beam neither diverges nor converges in the elevation plane. Since the horn is center mounted and normal to the elevation plane axis, the angular extent of the vertical plane is 84° and thus the desired 60°, 45°, and 37° beams can be supported by the reflector height of 36 inches, as shown in Figure 3-7. The dimensions of the primary apertures in the elevation plane needed to produce 37°, 45°, and 60° beamwidths were calculated to be 6.0", 5.0", and 3.7" respectively, for 4 kHz. These calculated values were validated by measurement. The taper of the horns should not exceed about 20° half angle. Thus, the length of the horn was roughly selected so that even with a 6-inch aperture, the taper would not exceed 20°. The horn length was chosen to constant at 8 inches.



AZIMUTHAL PLANE



ELEVATION PLANE

FIGURE 3-7. TRANSMITTING ANTENNA CROSS SECTION: AZIMUTH AND ELEVATION PLANES

Pipes, Flanges, Combiners, and Angles

Two Altec Lansing 290E drivers, each driven at ~ 100 watts average input power, are required to produce the desired acoustic drive to the primary aperture feed horn. The size and weight of these drivers (6.5" diameter, 30 lbs) would require a massive mounting structure, thus introducing considerable aperture blockage if mounted directly behind the feed horns. Consequently, it was decided to mount the drivers outside the secondary (parabolic cylinder) aperture and use pipes to transmit the acoustic energy to the primary aperture feed horn. The resulting transmission path length for each driver is approximately three feet. Figure 3-8 is a plot of the attenuation (resulting inside a circular pipe), in dB per foot versus acoustic frequency. The inside diameter of the pipe chosen was 1.43 inches, which resulted in an attenuation of about 0.75 dB for each path at 4 kHz. This inside diameter was also chosen because it matched the diameters of the driver throat and other available hardware (two-to-one combiner and angle bends) designed for use with the Altec Lansing 290E Driver. Figure 3-9 shows the details of the feed from the two drivers to the horn. The two elbows are Altec Lansing 45° bends (Model 30546). The two-to-one combiner is an Altec Lansing "Y" (Model 30170).

The efficiency of the entire feed structure, shown in Figure 3-9, was measured using both Altec Lansing 290E drivers and 291-16A drivers. The results are shown in Figure 3-10. The two drivers are comparable in efficiency with the 291-16's slightly better at both 3 kHz and 5 kHz and the 290E slightly better around 4-4.5 kHz. Since 4 kHz is the expected operating frequency and since the 290E can sustain higher input power, it was selected for use. In the frequency range of greatest interest, these curves predict an output of 30 acoustic watts, average, in the cw mode and nearly 60 acoustic watts, peak, in the pulsed mode of operation.

3.1.1.3 Transmitting Amplifier and Shelter

The remote transmitter electronics, as shown in Figure 3-11, consists of the Phase Linear Corporation Model 400 power amplifier used to drive the two transmit transducers and a signal splitter/power level control box. The amplifier has a nominal output rating of 200 watts/channel, rms, into the 8-ohm load of the Altec Lansing 290E driver. The drive level is controlled and balanced by adjusting the two potentiometers which control the signal level into each channel of the Phase Linear 400. Although lower drive level must be maintained for the cw mode of operation (100 watts, rms, continuous), the full 200 watts/channel may be utilized if necessary for the pulsed mode of

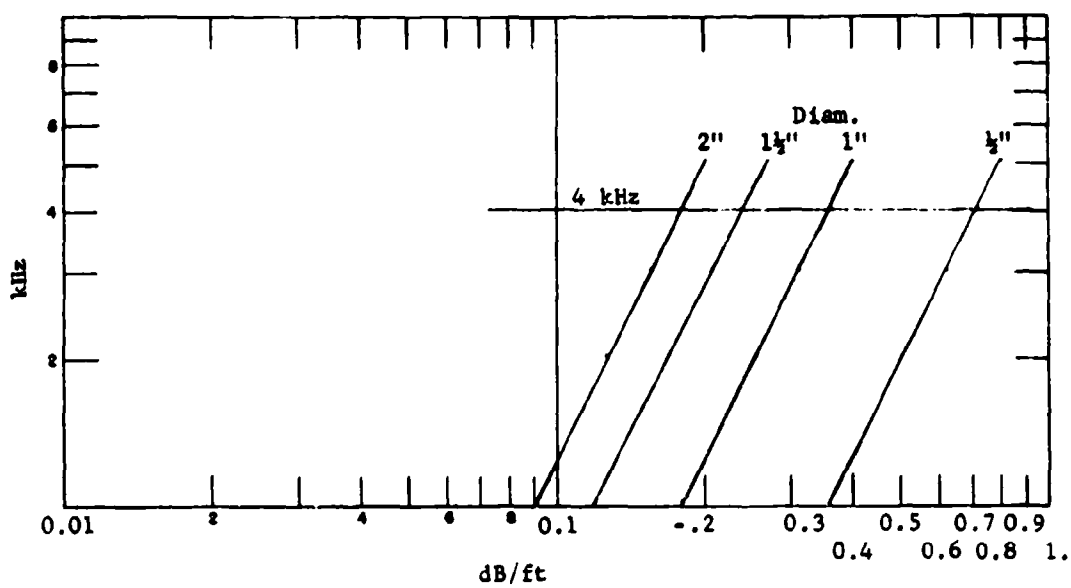


FIGURE 3-8. CIRCULAR PIPE ACOUSTIC ATTENUATOR CHARACTERISTIC

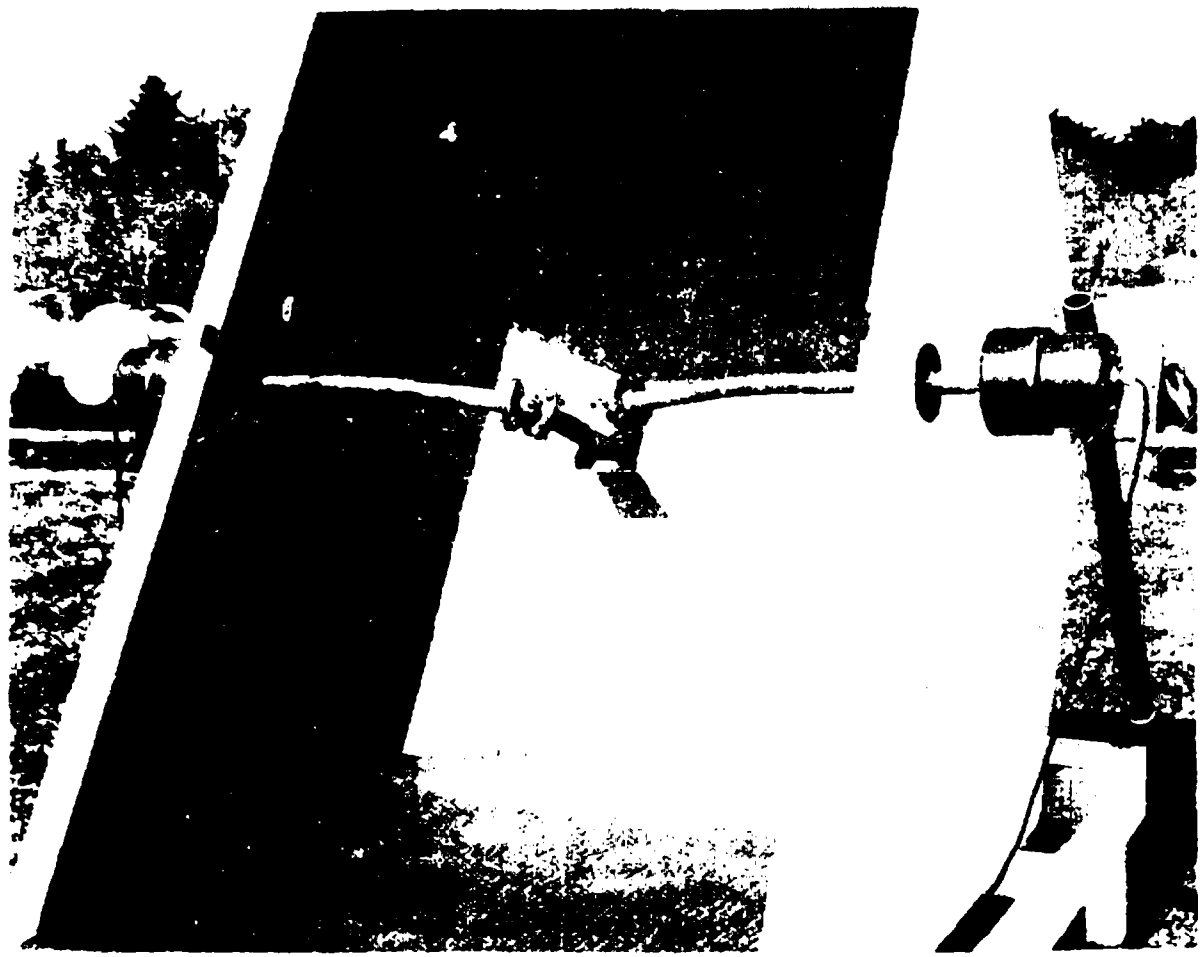


FIGURE 3-9. TRANSMITTER PHOTOGRAPH, SHOWING ACOUSTIC HORN-COMBINER FEED STRUCTURE

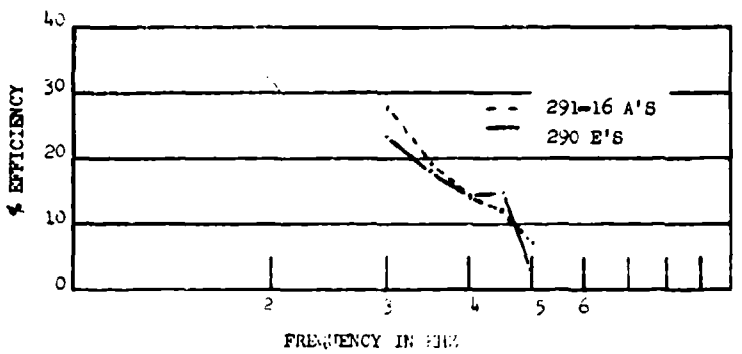


FIGURE 3-10. EFFICIENCY OF COMBINED OUTPUTS OF A PAIR OF ALTEC LANSING DRIVERS 290E's AND 291-16A's

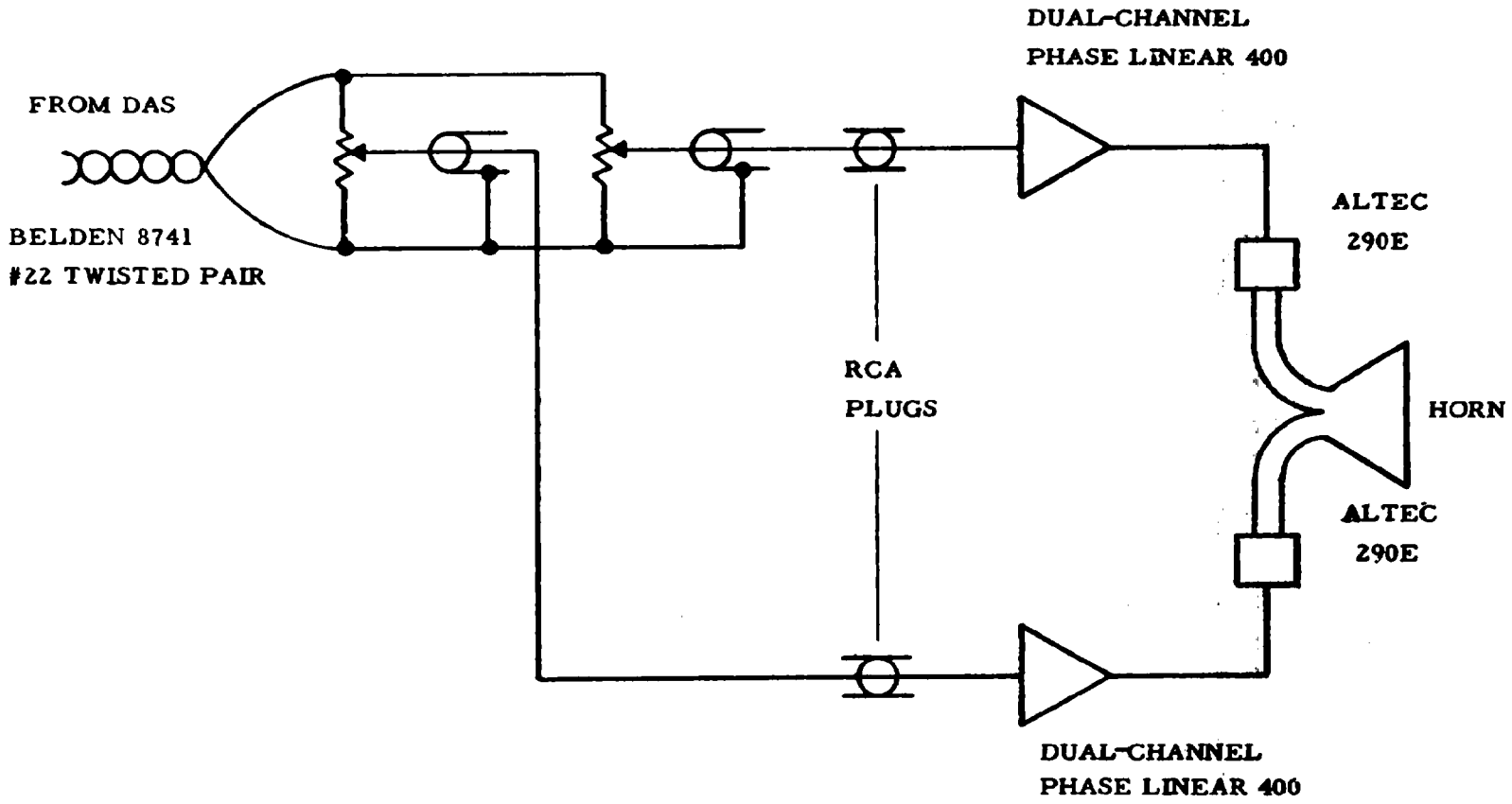


FIGURE 3-11. REMOTE TRANSMITTER ELECTRONICS

operation. Adjustment must be made manually at each remote transmitter site. The performance and specifications of the Phase Linear Model 400 amplifier are shown in Figure 3-12 and Table 3-4, respectively. The power amplifier is environmentally protected by application of Humiseal coatings to critical circuit areas. The housing used to protect the remote transmitting electronics from direct rain is a louvered enclosure, shown in Figure 3-13, typical of those used for weather instruments.

3.1.1.4 Signal and Power Distribution

As noted above, the transmitter signal cable is a single twisted pair #22 AWG shielded cable. The cable chosen actually provides two such pairs, one of which is reserved for a spare. The remote transmitting electronics require 117 volt, 60 Hz, 8 ampere, AC power with less than 5% drop. This primary AC power is provided at each transmitting antenna site. Figure 3-14 is a cabling and signal flow diagram for the remote transmitting antennas. The runs from the housed electronics (the DAS) to the remote antenna may be up to 5000 feet.

3.1.2 Receiving Antenna Assemblies

Each receiving antenna assembly, shown in Figure 3-15, consists of the following components:

1. Reflector, shroud, and support structure
2. Horn-microphone-receiver preamplifier subassembly
3. Signal and power distribution.

These major items are discussed in paragraphs 3.1.2.1, 3.1.3.2, and 3.1.2.3, respectively.

3.1.2.1 Reflector, Shroud, and Support Structure

The following paragraphs describe the acoustic design and the mechanical design of the reflector, shroud, and support structure.

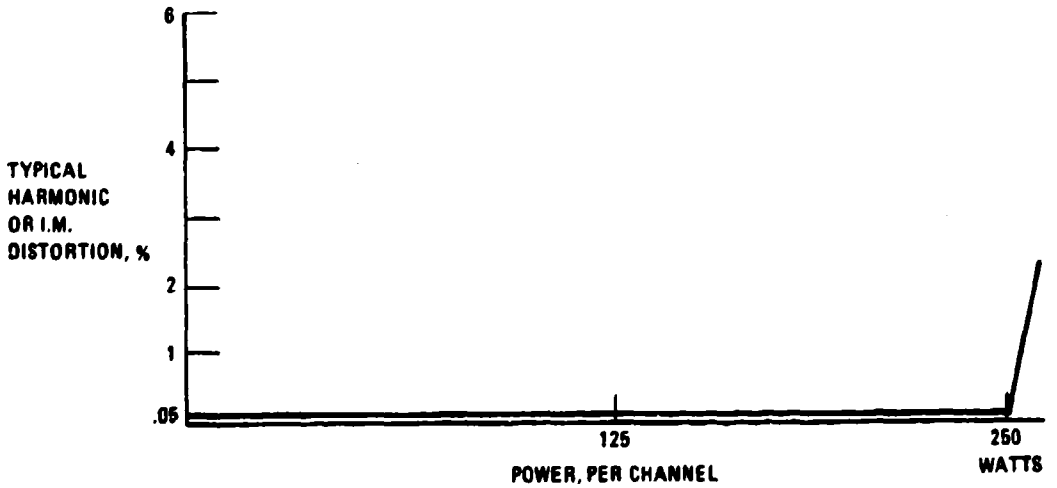


FIGURE 3-12. PERFORMANCE DATA - PHASE LINEAR 400 POWER AMPLIFIER

TABLE 3-4

PHASE LINEAR AMPLIFIER SPECIFICATIONS

POWER: Greater than 200 watts/channel, both channels driven into 8 ohms, zero to 20 kHz	PHASE SHIFT: Leading 0 degrees @ 20 Hz. Lagging 12 degrees @ 20 kHz
POWER AT CLIPPING: Typically 250 watts/channel, into 8 ohms, 400 watts/channel, into 4 ohms, 125 watts/channel, into 16 ohms	SENSITIVITY: 1.75 volts for 200 watts into 8 ohms
FREQUENCY RESPONSE: 0 to.25 MHz @ 1 watt	HUM AND NOISE: Better than 100db below 200 watts
HARMONIC OR INTERMODULATION DISTORTION: Less than .25%. Distortion is typically less than .05%	INPUT IMPEDANCE: 39 kilohms
DAMPING RATIO: Greater than 1,000: 1 @ 20 Hz	DIMENSIONS: 19 inches wide, 7 inches high, and 10 inches deep. Front panel bolt spacing will accommodate a standard rack mount
RISE TIME: Less than 1.7 microseconds.	FINISH: Light brushed gold, baked enamel, and black anodize.

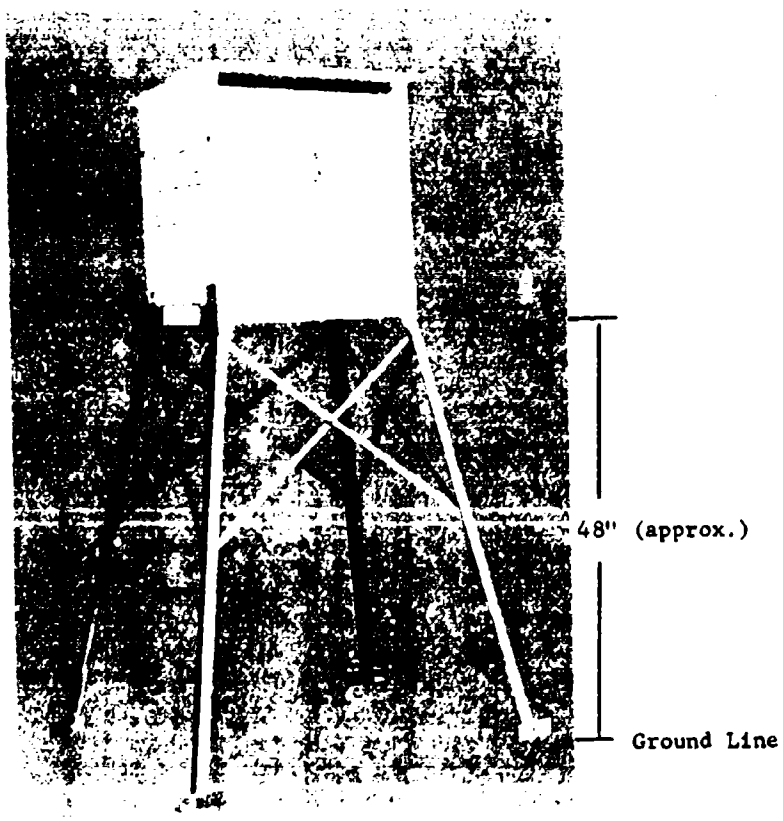
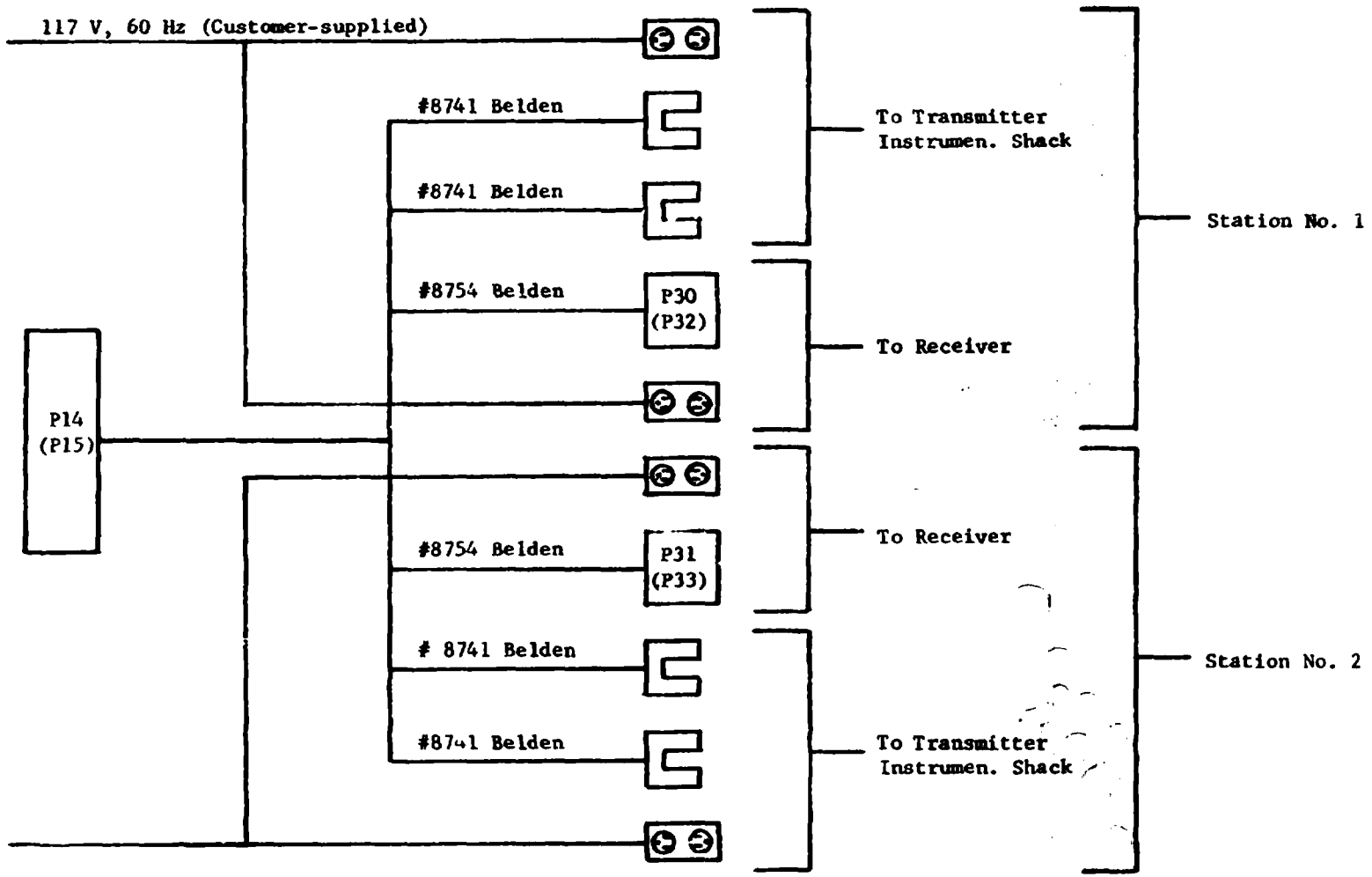


FIGURE 3-13. REMOTE TRANSMITTER ELECTRONICS ENCLOSURE



Note: P14 (P15) - Bendix PT06CE-24-61S(SR)
P30 (P32), and P31 (P33) - Amphenol 165-25

FIGURE 3-14. CABLING AND SIGNAL FLOW DIAGRAM

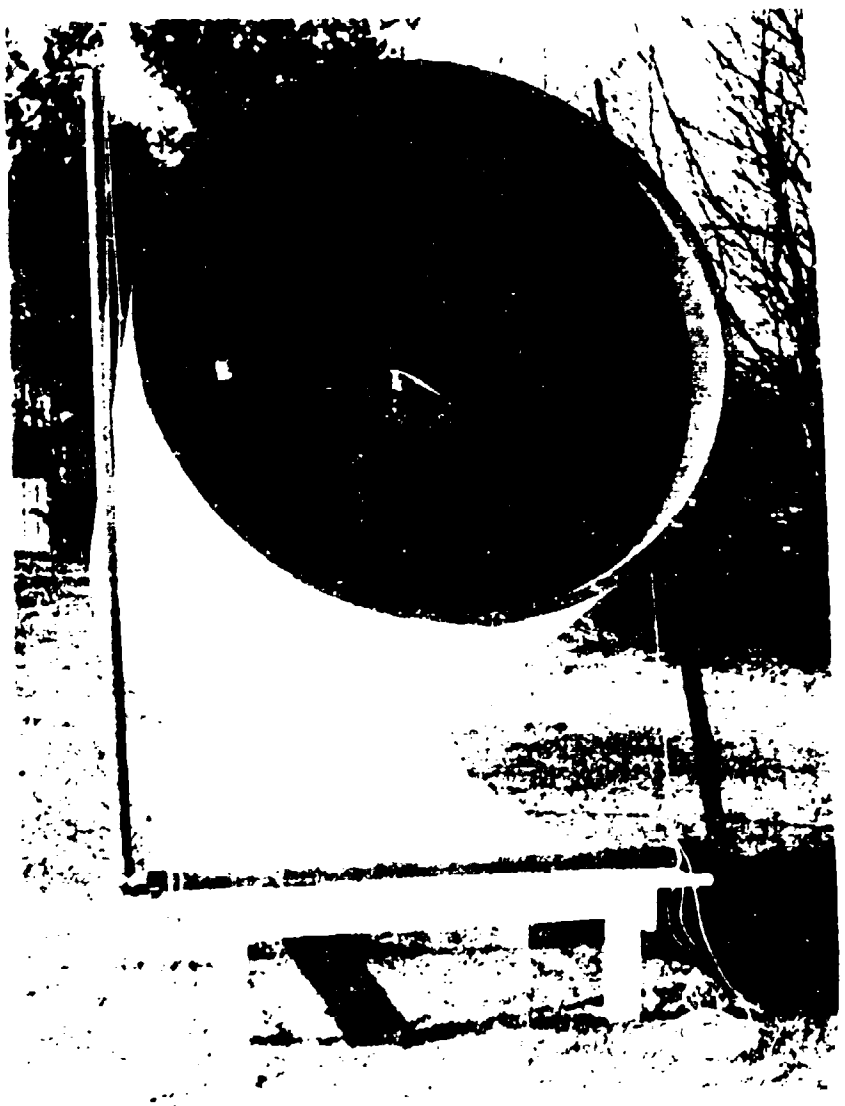


FIGURE 3-15. RECEIVING ANTENNA

Acoustic Design

The reflector and shroud design selected for the DAVSS receiving antenna assembly was chosen on the basis of: its ability to satisfy the acoustic radiation pattern requirements specified in Table 3-5, the field equipment environmental and physical design requirement listed in Table 3-2; and greatest commonality with already proven designs used by Avco in preparation for this DAVSS program. Initial measurements showed that a 6-foot diameter parabolic dish reflector with a 37-inch focal length yielded the nominal $3^{\circ} \times 3^{\circ}$ beamwidth desired when fully illuminated by a primary aperture. (Reciprocity between transmit and receive antenna beam patterns is assumed throughout; although all receive antenna measurements are actually made in the receiving mode.)

Experiments had been conducted at an urban airport prior to contract award using a 6-foot parabolic reflector fitted with alternative cylindrical shrouds of various lengths to reduce sidelobe response. The experiments indicated the necessity for a shroud length of nearly 8 feet and use of acoustic attenuation material as an inside liner of the shroud in order to reduce the airport environment background noise to acceptable levels.

The receiving antenna requirements called for the formation of a comb of twelve $3^{\circ} \times 3^{\circ}$ beams, each displaced by 3° from the next. This comb of receiver beams is realized in the design by arraying twelve (12) microphones across the focal plane of the parabolic dish. Shadowing of the parabolic dish would result from the shroud blocking some of the cross-section of incident rays for the off-axis beams. Theory predicts a lowering of the amplitude of the off-axis beams and a slight broadening of their principal beamwidth. To evaluate the expected shadowing effects, a full-scale reflector-shroud subassembly was constructed during the early design and test phase. It included a 12-channel microphone receiver preamp assembly mounted in the focal plane. The entire subassembly was mounted on a rotating table in Avco's anechoic chamber and the beam patterns in the principal planes of each microphone channel were measured at several frequencies in the 3-5 kHz range. The design goal was to achieve both the $3^{\circ} \times 3^{\circ}$ beamwidth at 4 kHz and to meet the following sidelobe requirement and goals:

	Requirement	Goal
Elevation	-25 dB for $20^{\circ} \geq \theta \geq 45^{\circ}$ -40 dB for $\theta \geq 45^{\circ}$	
Azimuth	-40 dB for $\phi \geq 90^{\circ}$	-50 dB for $\phi \geq 90^{\circ}$

TABLE 3-5

RECEIVING ANTENNA REQUIREMENTS

Design Parameter Requirements	Range
Frequency	f_o = 4.0 KHz 2.5 $\leq$ f $\leq$ 5.0 KHz
No. of Beams	12
Beamwidths (3 db)	
Elevation	3°
Azimuth	3°
Beam Elevation Coverage	$\pm$ 17° about boresight
Center Beam Adjustability	25° $<$ θ_c $<$ 90°
Sidelobes	
Elevation (θ)	-25 dB at $\pm$ 20° $\leq$ θ $\leq$ $\pm$ 45°
Azimuth (ϕ)	-40 dB at $\geq$ $\pm$ 45° -40 dB at $\phi \geq \pm$ 90°

Figure 3-16 shows the resulting elevation plane beam pattern and demonstrates the compliance with both sidelobe requirements and goals. Note the change of scale at $\pm 30^{\circ}$ in order to achieve the dynamic range in the test facility for sidelobe levels below -35 dB. The change of scale resulted from increasing the transmitter power by 30 dB beyond the $\pm 30^{\circ}$ points. A summary of the receiving antenna pattern results are shown in Table 3-6.

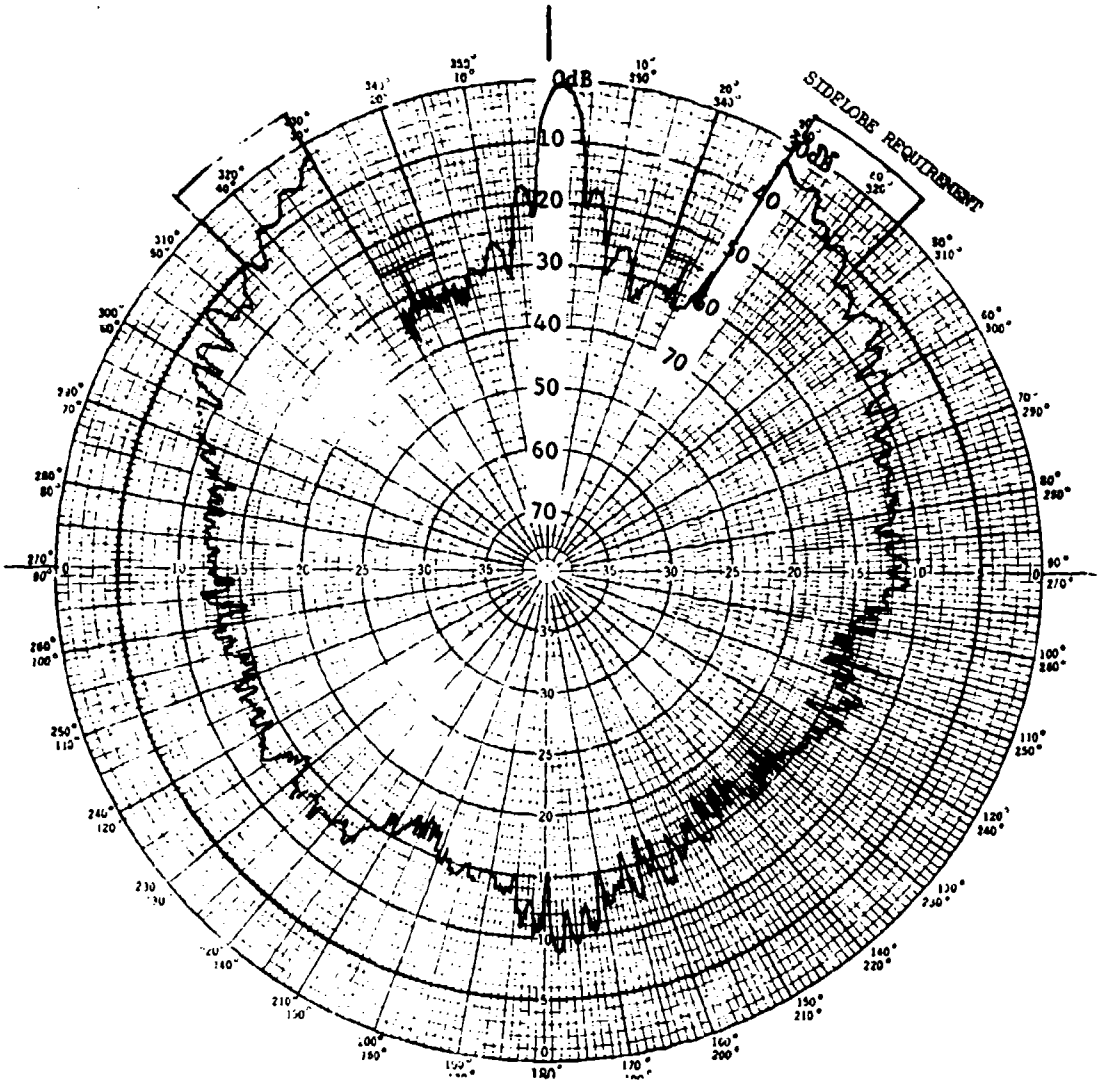
Mechanical Design

The reflector itself is 1/4-inch thick fiberglass formed into a parabaloid having a 6-foot diameter and a 37-inch focal length, as shown in Figure 3-17. The form is molded to a cylindrical shape around the circumference of the parabaloid in order to add rigidity to the structure and to provide a surface on which to bond the 6-foot diameter -- 8-foot altitude cylindrical shroud. To provide further stiffening, 3/4-inch ribs are contoured to fit the back of the dish and bonded at the seams of the shroud with screws and nuts and to the back of the dish with RTV-732. The ribs are symmetrically spaced at 72°. An extra vertical rib is also placed from the center hub to the bottom of the dish.

The microphone assembly is mounted on a quadripod of 1/2-inch conduit and is fastened to the parabolic reflector. The reflector surface is black. The pigment has been impregnated within the gelcoat to maintain a durable finish. Black was chosen to minimize the reflection and focusing of sunlight onto the microphone assembly, while retaining the smooth reflector surface for acoustic focusing.

The shroud is constructed in five identical 72° by 8-foot sections. Each section is constructed of a sandwich of 1/32-inch thick epoxy fiberglas, and 1-inch thick honeycomb (KP-1/2-6-25-E, Kraft), 1/32-thick epoxy fiberglas, and 1-inch thick Coustex absorber. The five sections are bolted together to form a cylinder. The parabolic dish is inserted in one end and bolted in place such that the ribs, the dish, and the seams of the shroud are bonded together. Several drain holes are bored in the dish to provide drainage of rain water. Holes are also bored in two of the quadripod feet and through the dish at these points to allow passage of both the signal cable and power supply cable.

The support structure is designed to allow the central beam to be adjusted in elevation from 0° to 90° above the horizontal. Figure 3-18 shows the receiving antenna assembly, including the support structure and tie-down scheme. The dish and shroud are so hinged that the barrel may be raised or lowered from a full down position (pointing



8-FOOT SHROUD

2-INCH APERTURE MINI-HORN

6-FOOT FIBERGLASS DISH

FEED NO. 7 OF 12

FIGURE 3-16. RECEIVING ANTENNA ELEVATION PLANE PATTERN, 4 kHz

TABLE 3-6

RECEIVING ANTENNA MEASUREMENTS

ELEVATION PLANE				
FREQ, kHz	BEAMWIDTH*		SIDELOBES*	
	REQ'D	MEAS'D	REQ'D	MEAS'D
3.0	-	4°	-	< -25 DB FOR 100% < -40 DB FOR 89% < -50 DB FOR 81%
4.0	3°	$3\ 1/2^{\circ}$	< -25 DB @ $\pm 20^{\circ}$ < -40 DB @ $\pm 45^{\circ}$	< -25 DB FOR 100% < -40 DB FOR 100% < -50 DB FOR 82%
5.0	-	$2\ 3/4^{\circ}$	-	< -25 DB FOR 100% < -40 DB FOR 100% < -50 DB FOR 83%
AZIMUTH PLANE				
FREQ, kHz	BEAMWIDTH		SIDELOBES	
	REQ'D	MEAS'D	REQ'D	MEAS'D
3	-	$3\ 3/4^{\circ}$	-	< -40 DB FOR 100% < -50 DB FOR 92%
4	3°	$3\ 1/4^{\circ}$	< -40 DB @ $\pm 90^{\circ}$	< -40 DB FOR 100% < -50 DB FOR 98%
5	-	$2\ 1/2^{\circ}$	-	< -40 DB FOR 100% < -50 DB FOR 100%

*BEAMS ADJACENT TO BORESIGHT ONLY

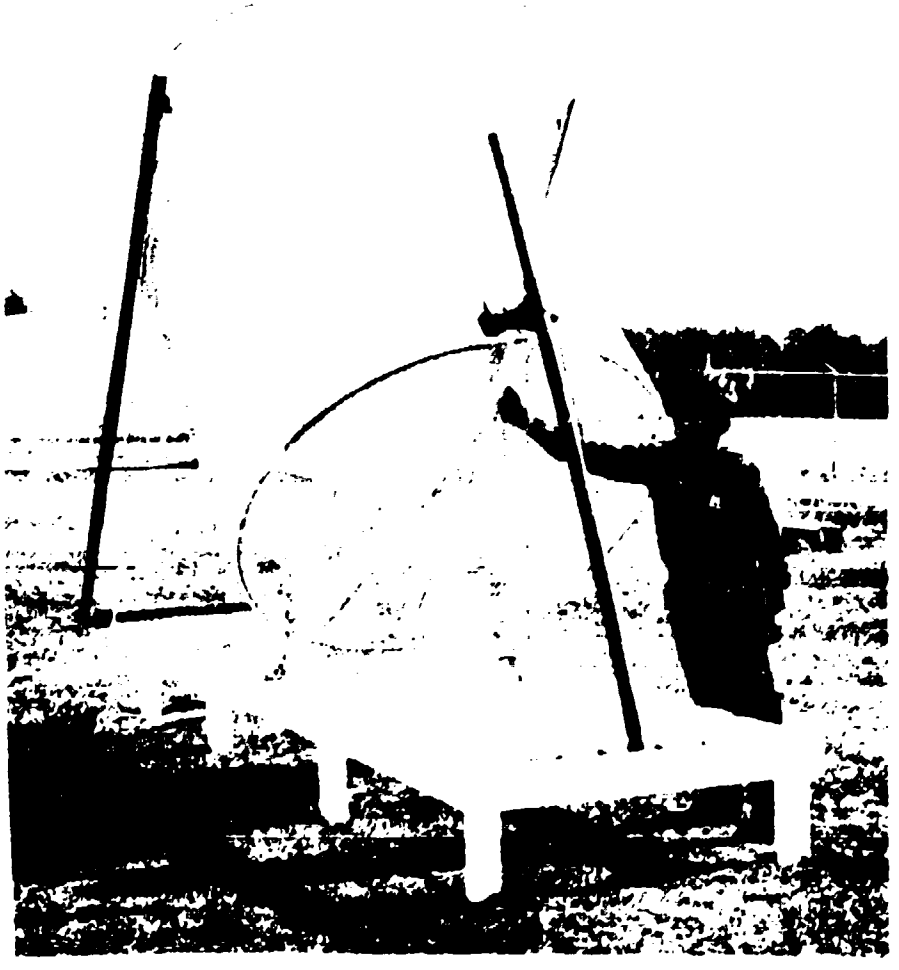


FIGURE 3-17. RECEIVING ANTENNA REAR VIEW AUTHOR IS CHECKING THE ELEVATION ANGLE OF THE ANTENNA.

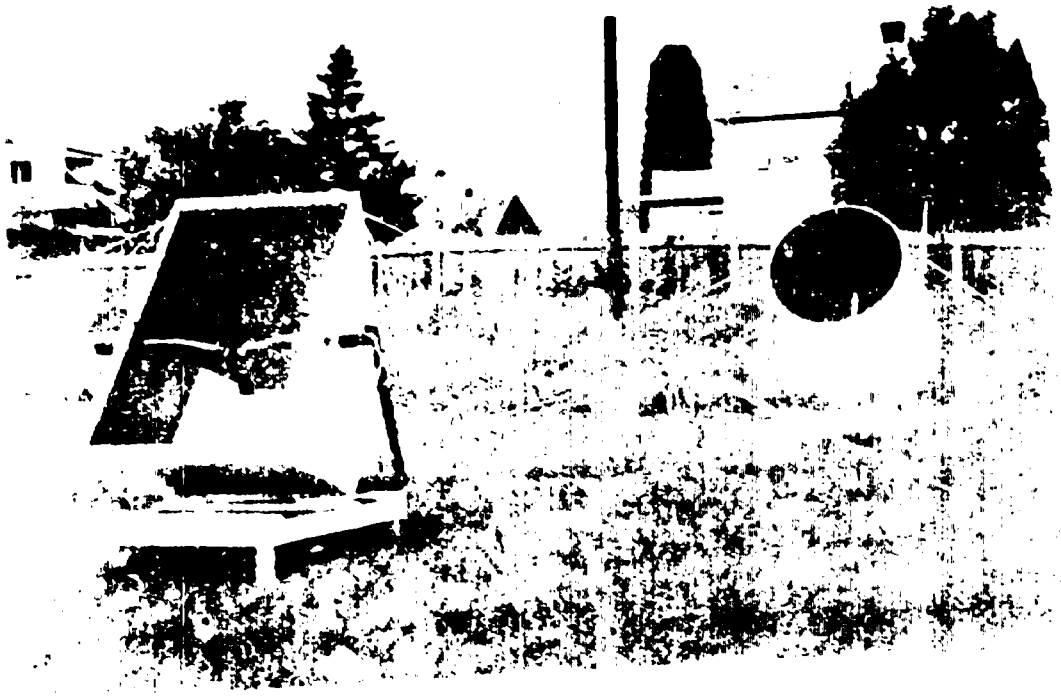


FIGURE 3-18. RECEIVING ANTENNA, SUPPORT STRUCTURE AND TIE-DOWN SCHEME

horizontally) to full up position (pointing vertically). The barrel is supported on each side and at the top rear by a PVC pipe and sleeve arrangement which is held in place by block type clamps. The forward support is a "U" shaped PVC pipe which is free to swivel in the elevation plane where it is supported on the front cross member of the six leg frame (earliest model shown in Figure 3-18 has eight legs). The rear support provides an angle brace and is also free to swivel in the elevation plane where it is supported on the back of the frame. The frame is constructed from 4" x 4", 2" x 8", and 2" and 6" lumber (for the legs, frame, and cross members, respectively).

Eyelets are provided at the front and rear top of the barrel and at 120° from the top center point on the front of the barrel for tie-down purposes. Dacron rope is secured from these points to four anchors set along diagonals to the stand, as shown in Figure 3-18. The tie downs must be loosened and retied for each adjustment of the antenna in the elevation plane.

3.1.2.2 Horn-Microphone-Receiver Subassembly

The horn-microphone-receiver subassembly is a single self-contained unit. It simultaneously forms twelve 3° x 3° beams displaced one from the other by 3° in the elevation plane and provides the acoustic-electrical transducers, preamplifier, and filter networks for the 12 receiver channels. The unit is environmentally sealed and has two watertight connectors: one for the external power supplies and the second for the multi-pair signal output cable. The assembly is approximately 28.5" long by 2" wide by 5.5" high. It has 12 Delrin mini-horns which provide the impedance matching to each of 12 miniature condenser microphones. Each microphone drives its own filter and preamplifier network. Figure 3-19 shows the horn-microphone-receiver subassembly.

The following paragraphs describe first the acoustic design and then the mechanical design of the horns, microphones, the mini-horns, the receiver, and the subassembly itself.

Microphones

In order to achieve the scan comb requirement of twelve 3° x 3° beams separated by 3° in the elevation plane, the twelve microphones must be arrayed across the focal plane of the parabolic reflector dish with a center spacing of about 2 inches.

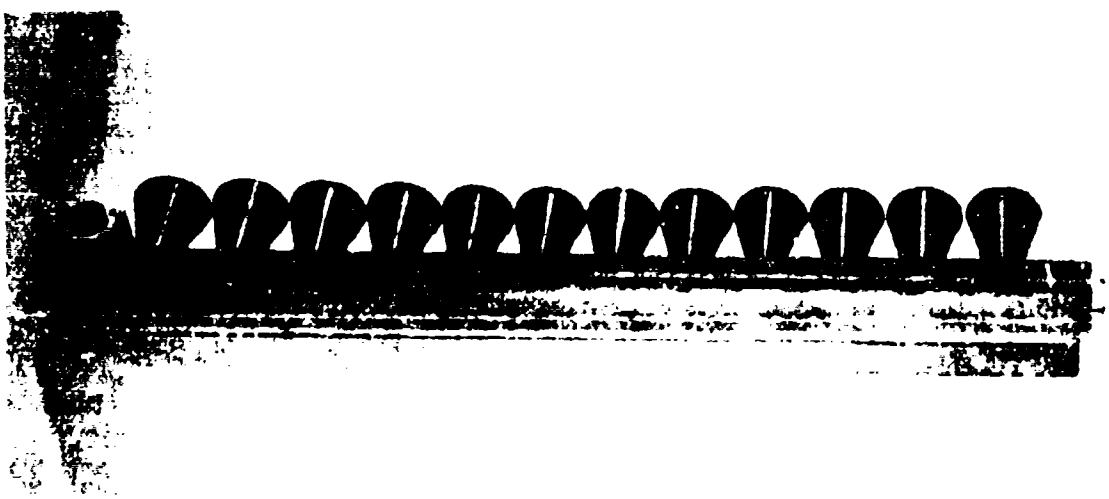


FIGURE 3-19. HORN-MICROPHONE-RECEIVER SUBASSEMBLY

The microphone selected for the receiver is a Thermo-Electron miniature condenser microphone, Model 5336C. This microphone, complete with an FET source follower, has the following characteristics:

Sensitivity	-61 dB V (re: 1 V/ μ bar)
Noise Level	29 dB SPL (-13 dB/ $\sqrt{\text{Hz}}$)
Output Impedance	1000 to 2500 ohms
Frequency Response	50 to 16,000 Hz
Supply Voltage	8 to 30 V
Current Drain	1 ma
Dimensions	0.280 x 0.280 x 0.160 inches
Distortion (5% THD)	140 dB SPL

The unit has sintered metal terminations and is weatherproofed. It also exhibits very low susceptibility to vibration and high resistance to damage from shock. Tests have shown that the microphone's sensitivity is virtually unaffected by continual storage at 50°F and 94% relative humidity without sealing or protection. Its small size and rugged characteristics allowed the greatest flexibility in the design of the horn-microphone-receiver subassembly itself.

Mini-Horns

The miniature microphone's small size insures an almost omnidirectional pattern. Its effective aperture is 0.190 inches in diameter, or 0.03 square inch. It was found that the over-all gain of the microphone could be improved by mounting a mini-horn in front of the sensitive aperture of the microphone. This resulted in a small change in the element pattern -- a change that was also desirable because it provided some additional directivity. Figure 3-20 shows the beam patterns and relative gains of various sizes of mini-horns versus those of the microphone without a mini-horn, as measured at 4 kHz. Figure 3-21 shows the variation with frequency of the relative gain of 1, 1.5, and 2-inch mini-horns with respect to the microphone alone (electret). Over the frequency range required, the 2-inch mini-horn was the best choice for the flatness of relative gain versus frequency, relative gain, and 3 dB beamwidth. Consequently, the horn, microphone, receiver sub-

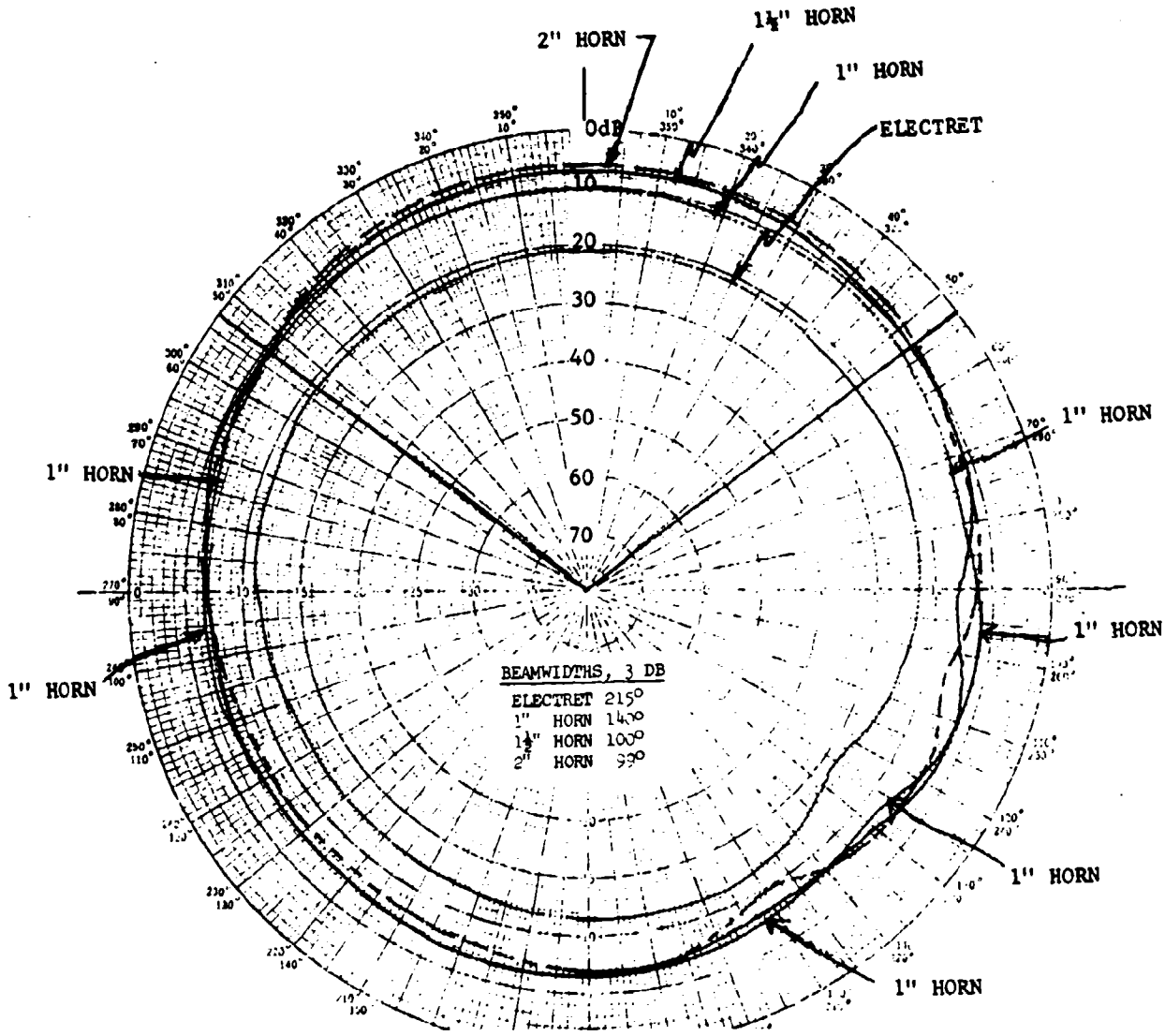


FIGURE 3-20. MINI-HORN BEAMWIDTHS AND RELATIVE GAIN AT 4 kHz

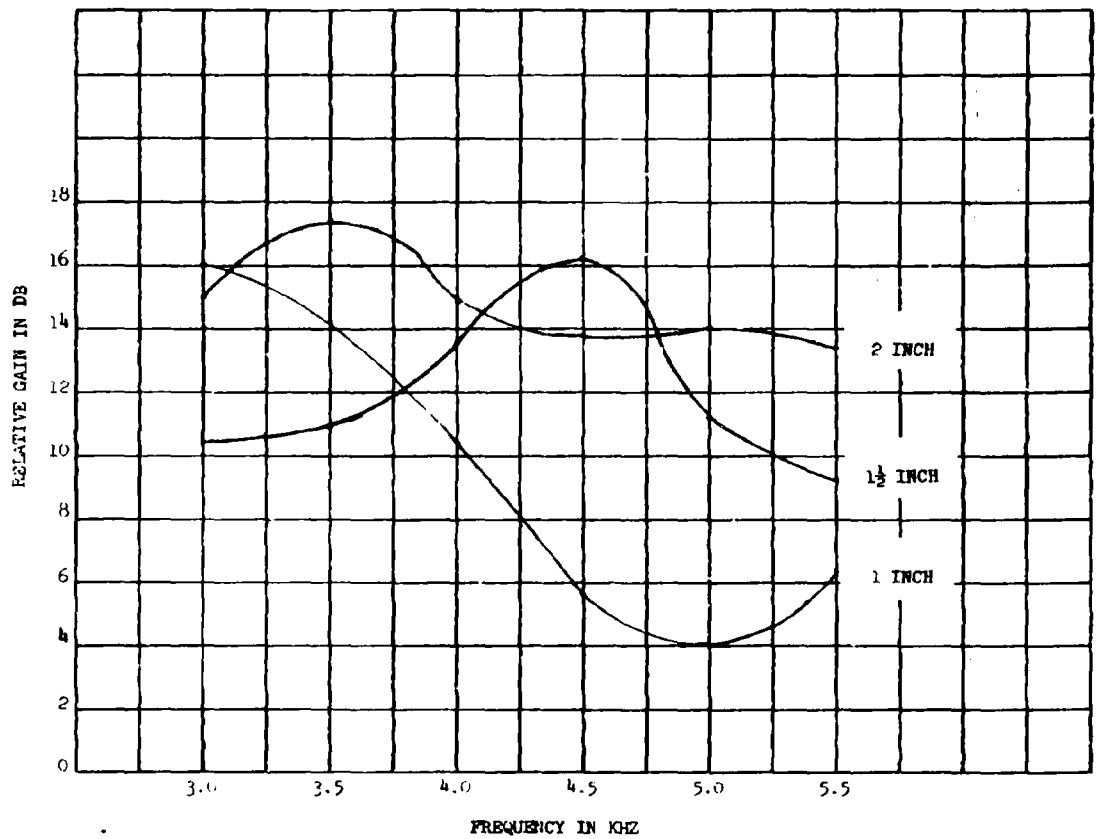


FIGURE 3-21. GAIN OF 1", 1-1/2", AND 2" APERTURE MINI-HORNS VERSUS FREQUENCY RELATIVE TO ELECTRET WITH NO HORN

assembly utilizes 2-inch (nominal) aperture mini-horns in front of each of the 12 electret microphones to increase their gain by about 14 dB, minimum, and to more nearly match their primary beam shape to that desired for illumination of the parabolic dish reflector. The actual horns are tailored for their individual position within the 12-microphone array with the aperture size increasing as a function of their displacement from the array center. Thus, the outer horns for beams 1 and 2 and 11 and 12 are slightly larger and have slightly greater gain than the center horns for beam 5, 6, 7, 8, etc. All the horns are coded and marked as to their proper position within the subassembly.

The Delrin horns are turned on a lathe to a conical shape and threaded to allow mounting into the base block of the microphone receiver subassembly. Each horn is nominally 3 inches in length with a 2-inch aperture. The taper is brought down to match the 0.190 inch diameter of the sensitive portion of the electret microphone.

Receiver Preamplifier

To improve the signal-to-noise performance and reduce the system's susceptibility to electromagnetic interferenc. (because of the long signal lines between the receiver site and the data acquisition subsystem), about 80 dB of preamplification and pre-filtering is provided in each of the 12 signal lines within the horn-microphone-receiver subassembly. Figure 3-22 is a schematic diagram of the preamplifier circuit. As the schematic indicates, each electret microphone derives its power from the common 15V supply. The microphone is immediately followed by a high-pass network whose cut-off frequency is chosen to reduce the low frequency spectrum where most of the noise power lies. This high pass network is followed by two stages of amplification, the second stage of which can be manually adjusted by a 0-0.5 megohm potentiometer. The final stage is a line drive power amplifier capable of driving the long twisted pair signal line used to carry the signal back to the data acquisition system.

Three receiver preamplifier circuits are located on each of four printed circuit (PC) boards. These four boards are mounted behind the horn and microphone plate, as shown in Figure 3-23. The entire subassembly is environmentally sealed with the rubber gasket and cover.

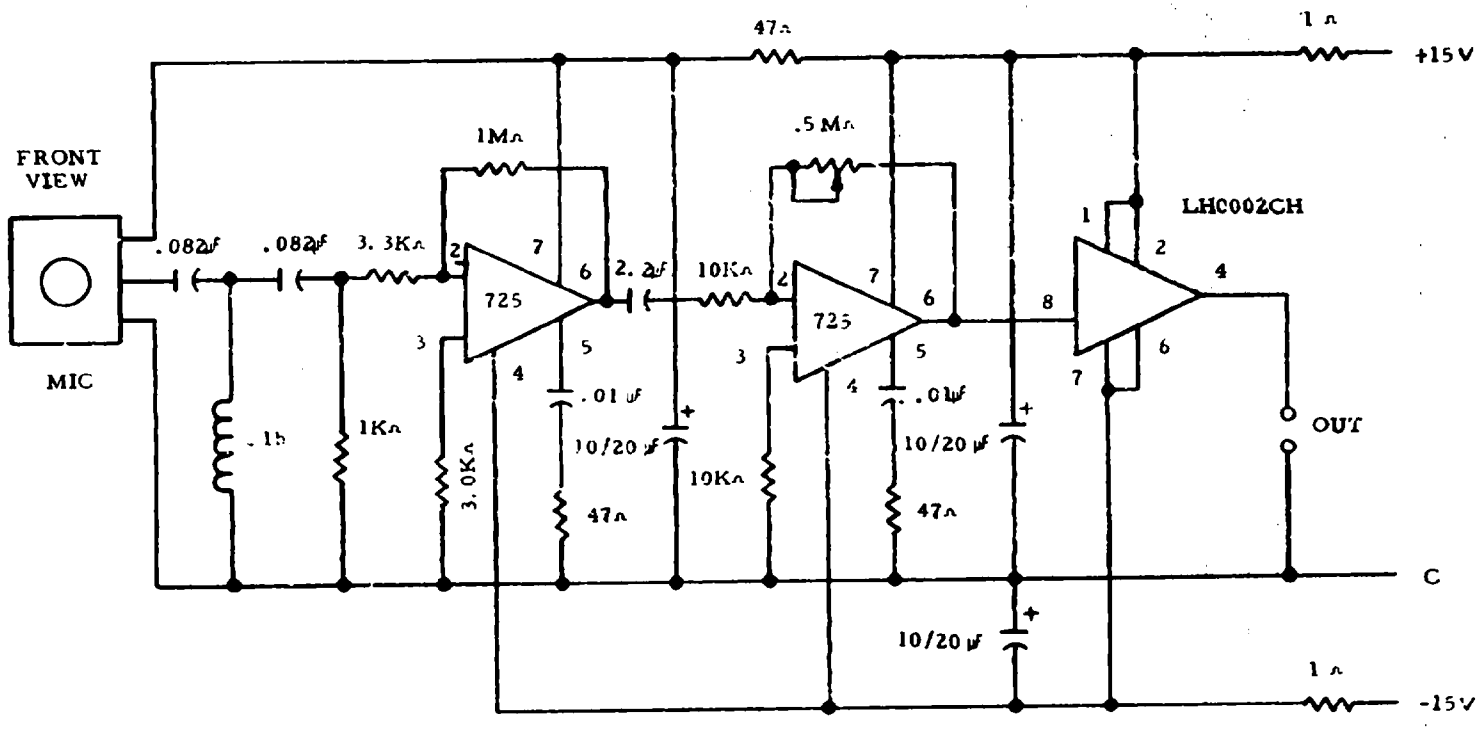


FIGURE 3-22. DAVSS RECEIVER PREAMPLIFIER

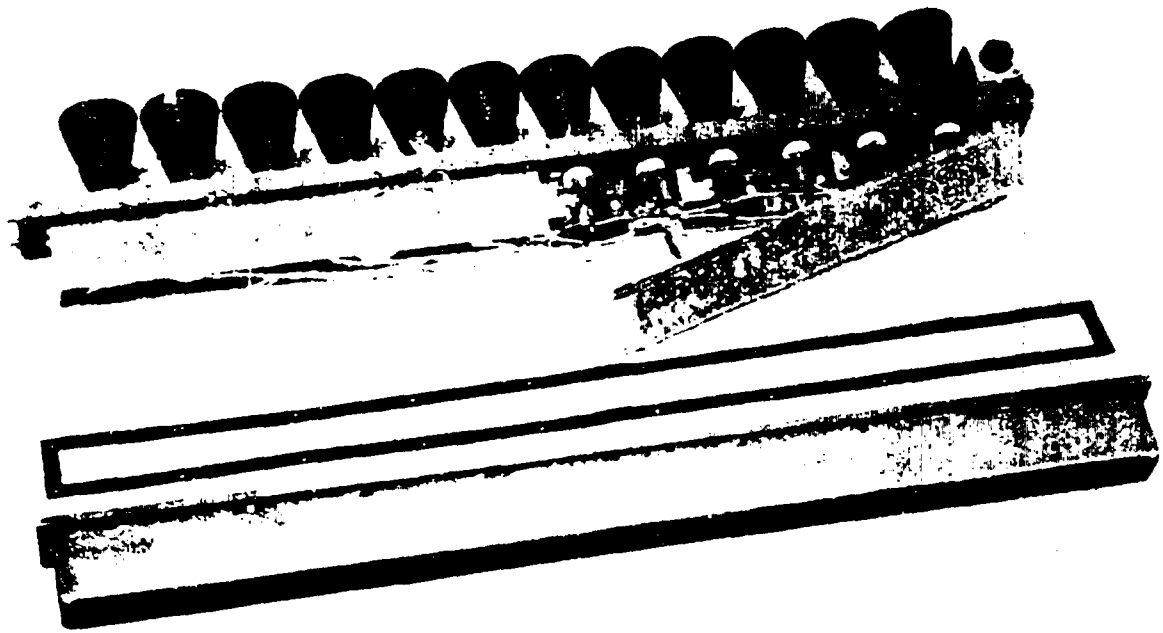


FIGURE 3-23. PARTIALLY DISASSEMBLED HORN-MICROPHONE-RECEIVER SUBASSEMBLY

Receiver Subassembly and Housing

The receiver subassembly and housing is designed: (1) to place each individual horn and microphone in the proper position in the parabolic plane to form a receiver beam at the desired angle with respect to the axis of the reflector itself, and (2) to provide an environmentally sealed volume to house the preamplifiers, filters, and line drivers. Two water-tight Amphenol connectors are provided: one to carry +15 volts, and common from the power supply (which is mounted behind the reflector), the second to connect the 12 microphone signals via a 13-pair (twisted) cable to the data acquisition subsystem.

The housing itself consists of a base plate, rubber grommet, cover, and mounting brackets. The base plate is a 1" x 2" x 28" aluminum block which is drilled and tapped to allow the twelve threaded mini-horns to be screwed in. At the bottom of each tap, a tapered hole is bored to continue the horn taper to the sensitive aperture of the microphone.

The microphones themselves are each mounted in a phenolic disk which is attached by four screws to the back of the base plate behind each horn. The disks are provided with three pins to permit electrical connection of the microphone (via a Berg connector) to the electronic printed circuit boards. The four printed circuit boards are mounted by brackets to the back of the base plate, as shown in Figure 3-23. Individual twisted pairs connect the output of each receiver preamplifier channel to the mounted male Amphenol connector. The welded aluminum cover is placed over the electronics on top of the rubber grommet and secured in place with 20 Allen-head machine screws.

The mounting brackets (two) are attached to the upper and lower end of the receiver subassembly and each bracket mounts on one of the two tubular bi-pods. A set of three rubber bushings in each mounting bracket reduces microphonic pick up of vibrations entering the microphone-receiver assembly from the receiver dish assembly itself.

A single adjusting bar is provided to control the vertical position of the subassembly within the dish under the varying loads which result from the 90° variation in elevation of the axis of the dish itself.

3.1.2.3 Receiver Antenna Measurements

Measurements were made of the antenna beams achieved by the actual receiver assembly described in paragraphs 3.1.2.1 and 3.1.2.2 above. Figures 3-24, 3-25, and 3-26 show the resulting multiple beam pattern at 3, 4, and 5 kHz, respectively. Figure 3-27 shows the relationship of the 3 dB beamwidth versus beam position for the three frequencies of interest. The increase in beamwidth with off-axis displacement is due in part to the obscuration of the dish by the shroud. It is considered acceptable, however.

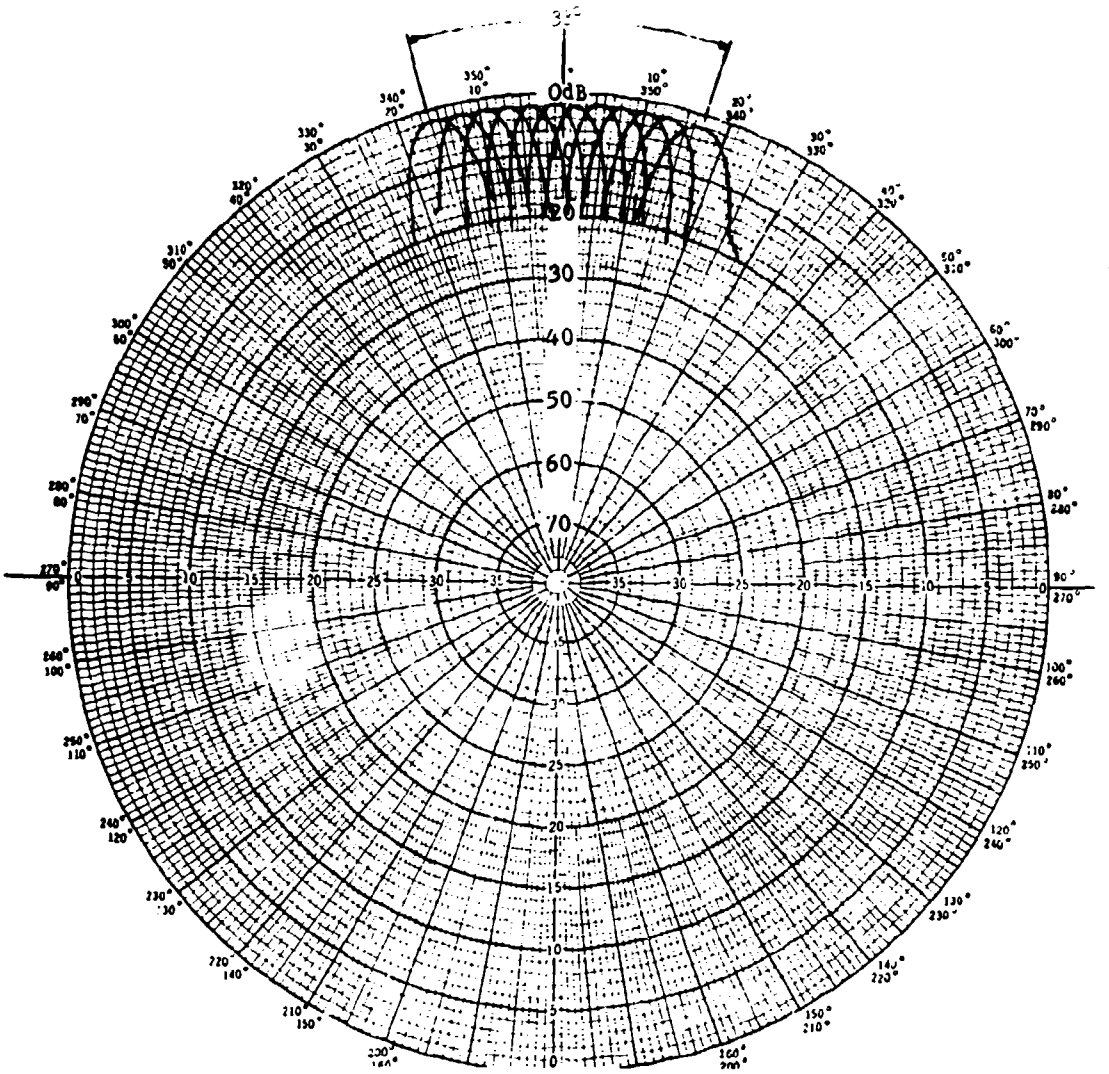
Figure 3-28 is a plot of the first sidelobe amplitudes as a function of beam position at 4 kHz. It shows that the sidelobe toward the axis of the dish increases with increased displacement from the center beam while the sidelobe away from the center decreases. However, the total variation is less than 6 dB and no sidelobes are higher than -15 dB with respect to main beam.

3.1.2.4 Receiver Signal and Power Distribution

Twelve channels of received signals must be carried from each receiving antenna assembly to the data acquisition subsystem; and primary power must be delivered to each receiving antenna assembly for the $\pm$15V supplies of the horn-microphone-receiver subassembly. The signal cable contains 13 twisted and shielded pairs of #22 wire in a Belden 8754, or equivalent, cable. One pair is reserved as a spare. The connector at the horn-microphone-receiver subassembly is a waterproof-type Amphenol 165-25 female connector which connects into the corresponding male connector mounted on the assembly. The cable runs through the back of the dish through an enlarged hole which may be reached by temporarily removing one of the quadripod flanges from the dish.

The two 13-pair cables from the two receiving antenna assemblies in one array and the two 2-pair cables from the two transmitting antenna assemblies in the same array are all joined in a common Bendix connector which connects into the isolation module at the data acquisition subsystem.

The primary power required to be supplied is 117 volts, 60 Hz, and 1 ampere with regulation of $\pm$5% or better. It terminates in a flexible cable at the bottom rear of the receiver shroud with a standard outdoor-type 3-prong duplex receptacle mounted on the shroud brace. A separate +15V power supply is a part of the receiving antenna assembly and is

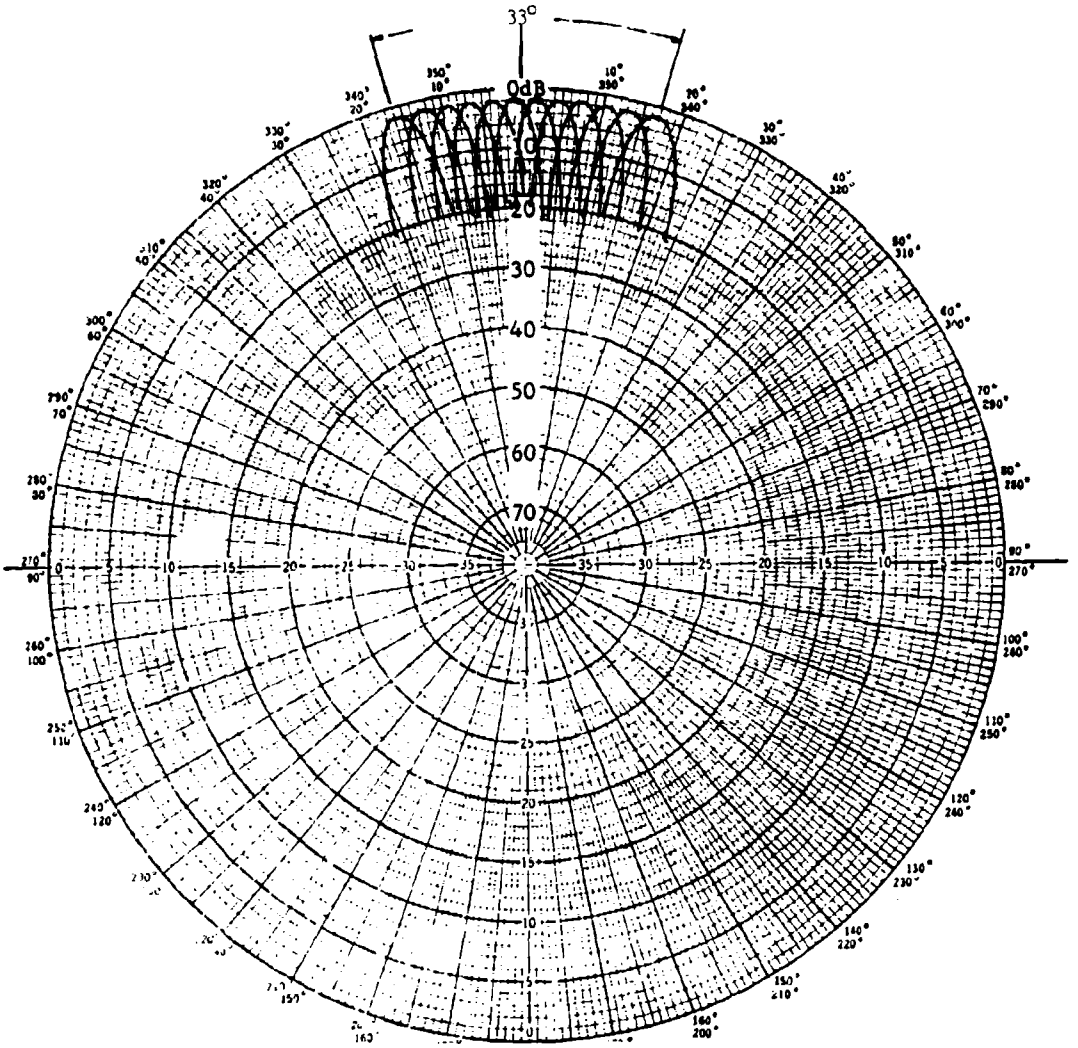


8-FOOT SHROUD

2-INCH APERTURE MINI-HORN

6-FOOT FIBERGLASS DISH

FIGURE 3-24. RECEIVING ANTENNA: MULTIPLE ELEVATION BEAM PATTERN AT 3 kHz

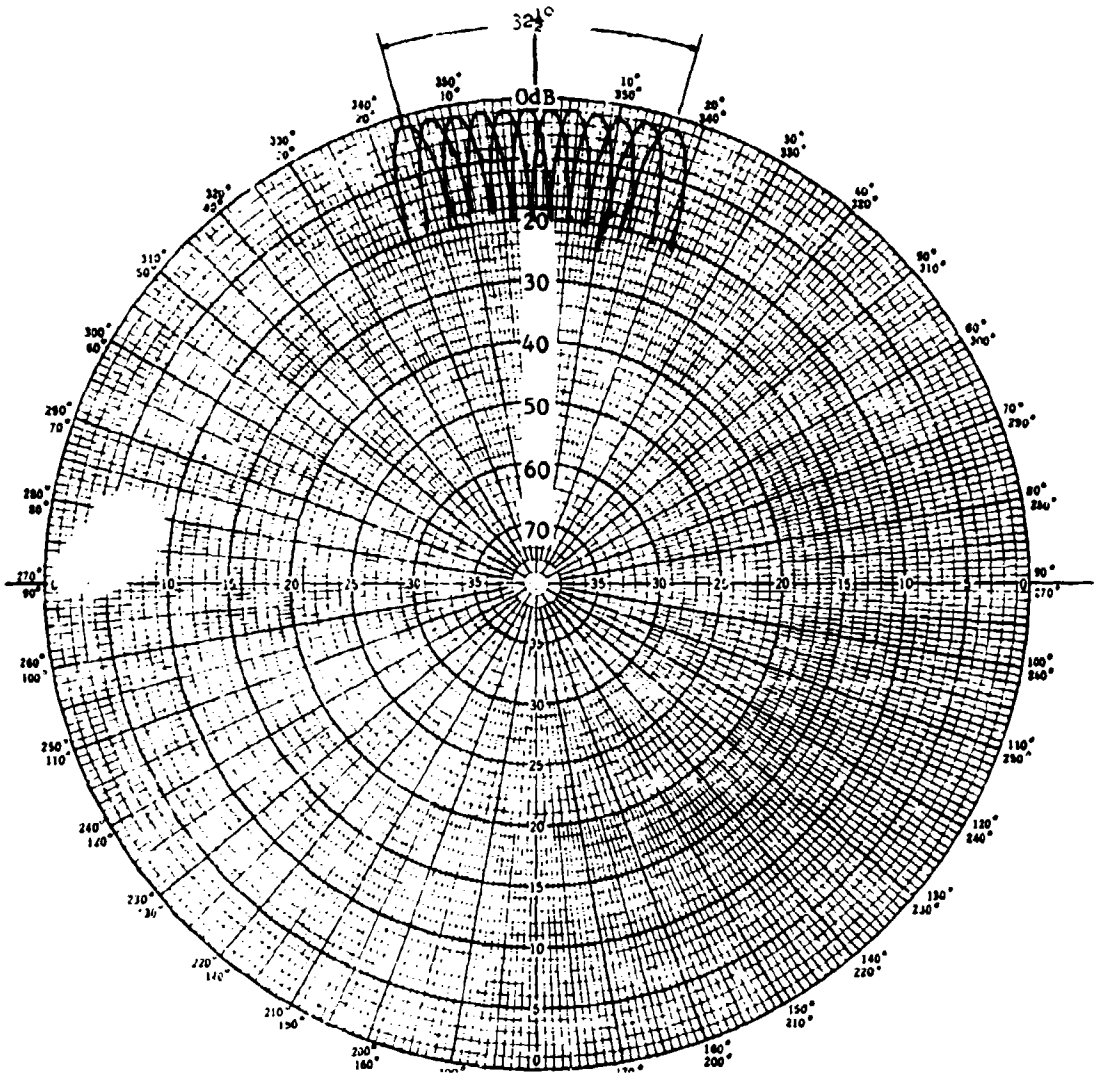


8-FOOT SHROUD

2-INCH APERTURE MINI-HORN

6-FOOT FIBERGLASS DISH

FIGURE 3-25. RECEIVING ANTENNA: MULTIPLE ELEVATION BEAM PATTERN AT 4 kHz



8-FOOT SHROUD

2-INCH APERTURE MINI-HORN

6-FOOT FIBERGLASS DISH

FIGURE 3-26. RECEIVING ANTENNA: MULTIPLE ELEVATION BEAM PATTERN AT 5 kHz

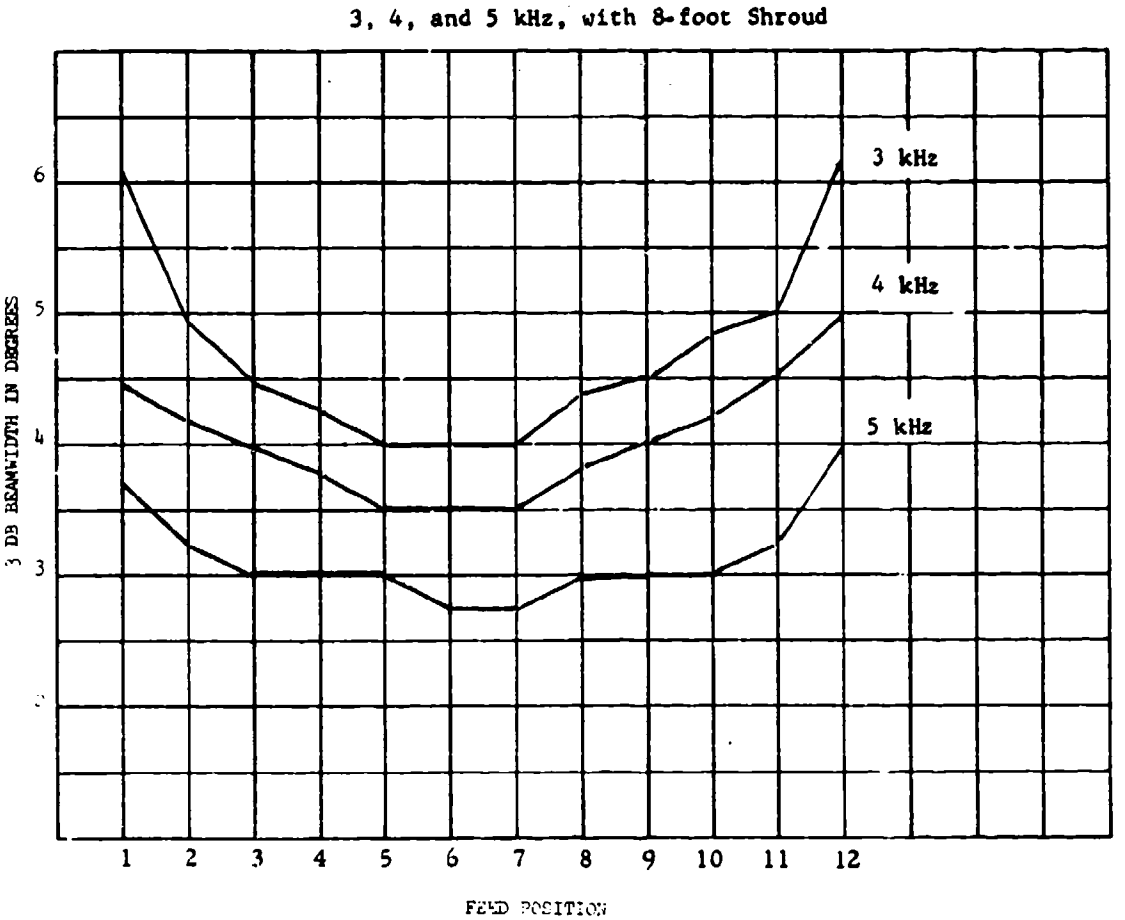


FIGURE 3-27. RECEIVING ANTENNA: BEAM WIDTH VERSUS BEAM DISPLACEMENT

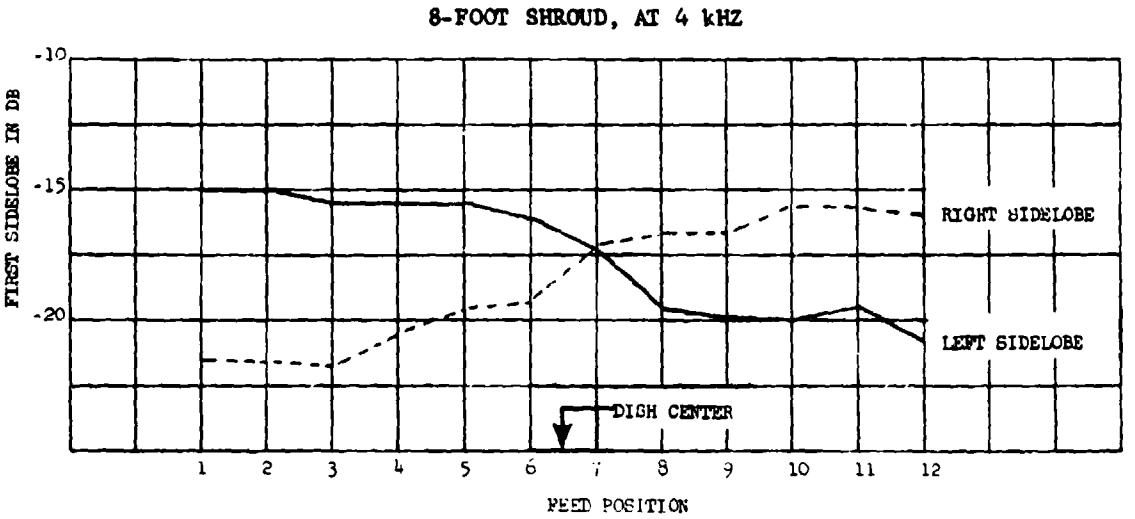


FIGURE 3-28. RECEIVING ANTENNA: SIDELOBE VALUE VERSUS FEED POSITION

mounted under a rain cover on the top back of the reflector dish. A single cable leads from this power supply through a hole in the dish beneath the other top quadripod flange to the power supply Amphenol connector on the horn-microphone-receiver subassembly.

3.1.3 System Signal and Power Distribution

The signal and power distribution scheme for one array of the DAVSS is shown in Figure 3-14. The distribution scheme for the second array is identical to the first, except the connectors are as labeled in the parentheses. Each array is connected to a separate part of the isolation module via connector P14 (P15). Four separate cables are joined in this connector: two 13-pair cables to the two receiving stations and the two 2-pair cables to the two transmitting stations in each array. A transmitter (2-pair) cable and a receiver (13-pair) cable are run together to the point near the transmitter and receiver where the customer-supplied 117V, 60 Hz primary power distribution box is located. At this point, the 2-pair transmitter cable is run into the transmitter instrument shelter and the 13-pair receiver cable is run directly to the rear of the receiving antenna where it is passed through an access hole in the reflector to the horn-microphone receiver subassembly. The transmitting signal pair is connected to a signal splitter and equalizer circuit from which two signal lines are used to drive the two channels of the Phase Linear amplifier. The two output lines from the dual channel amplifier are run directly to the two Altec Lansing 290E electro-acoustical transducers.

Primary power distribution lines are run from the 117V, 60 Hz distribution box to the transmitter instrument shelter and to the rear of the receiving antenna assembly where the horn-microphone receiver subassembly power supply located on the top rear of the reflector is connected.

In general, four such installations are required for the four pairs of transmitters and receivers. In practice, however, one array is scheduled for bistatic operation and the other array for monostatic backscatter operation. In this configuration, the monostatic backscatter stations are collocated and the amplifiers for two transmitters are installed in the same transmitter instrument shelter and only one primary power distribution point is located next to it.

For protection against hazard from machine and animals, all cable runs are buried to the greatest extent possible, and where not buried they are held off the ground.

3.2 DATA ACQUISITION SUBSYSTEM

The (DAVSS) Doppler acoustic vortex sensing system is shown in block diagram form in Figure 3-29. Descriptions of various items included in the data acquisition subsystem (DAS) follow.

3.2.1 Isolation Module

The isolation module: (1) provides galvanic isolation between the data acquisition equipment and the cables to the Doppler acoustic radar antennas, and (2) protects the signal processing equipment from overvoltage surges originating in the external cabling. Lightning arresters in the form of neon bulbs, added to each leg of the transformer, afford the system some lightning protection. Signals from the receive antennas are pre-filtered through passive high-pass filters to eliminate high-amplitude, low-frequency noise that might saturate the active components in the signal processing chain.

The basic circuit of this module is shown in schematic diagram form in Figure 3-30.

3.2.2 Configuration Control Module

The configuration control module contains the switching matrix and associated control circuits used to interconnect the inputs and outputs of the data processing circuits, the analog tape unit, and the two Doppler acoustic radar arrays. The system configuration is represented by an 8-bit code as shown below:

CONFIGURATION CONTROL

Bit	Purpose
15-6	Not Used
5	TRANSMITTER-2 FREQUENCY SELECT
	0 = FREQ 1 1 = FREQ 2
4	TRANSMITTER-1 FREQUENCY SELECT
	0 = FREQ 1 1 = FREQ 2

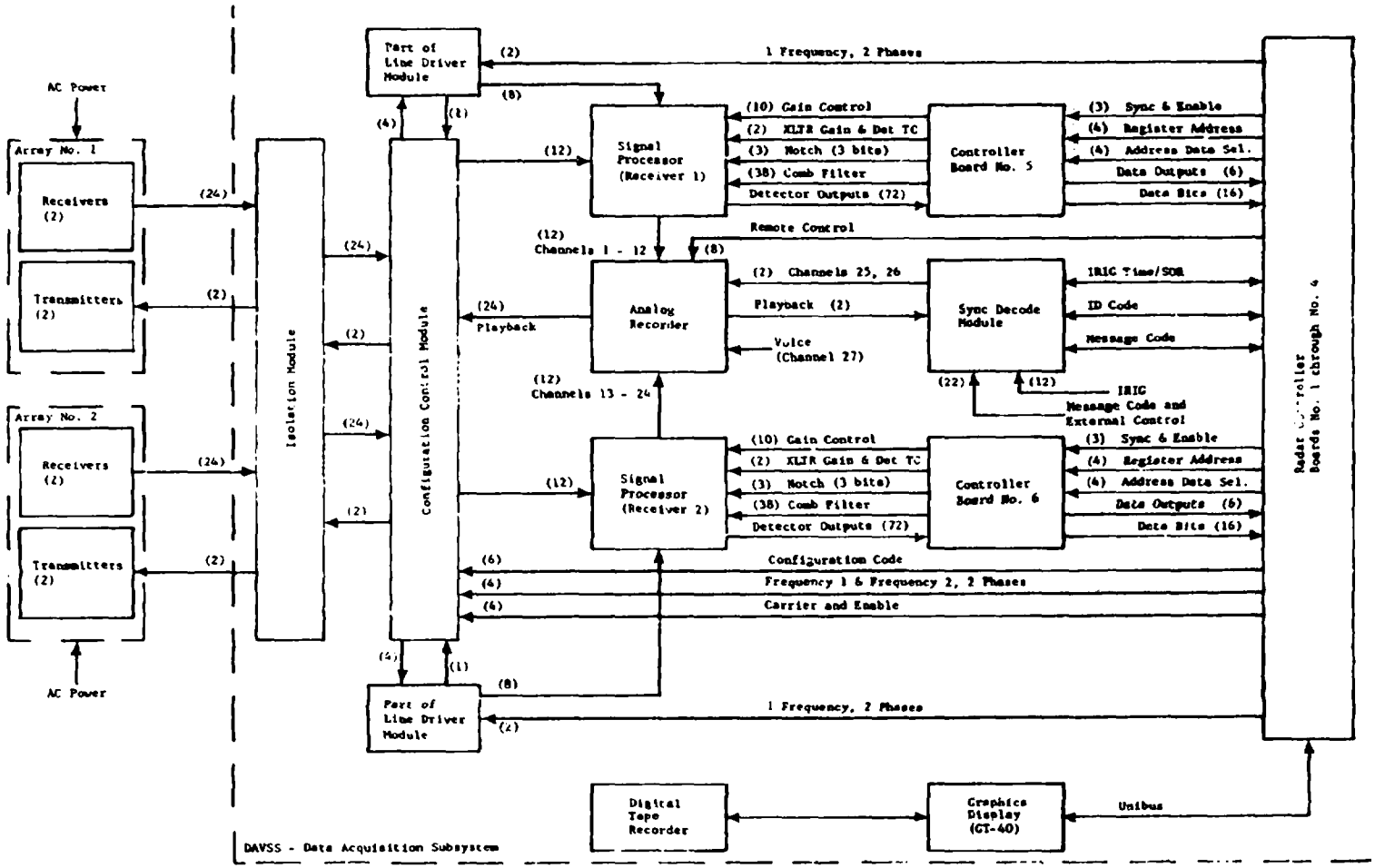


FIGURE 3-29. BLOCK DIAGRAM OF DAVSS

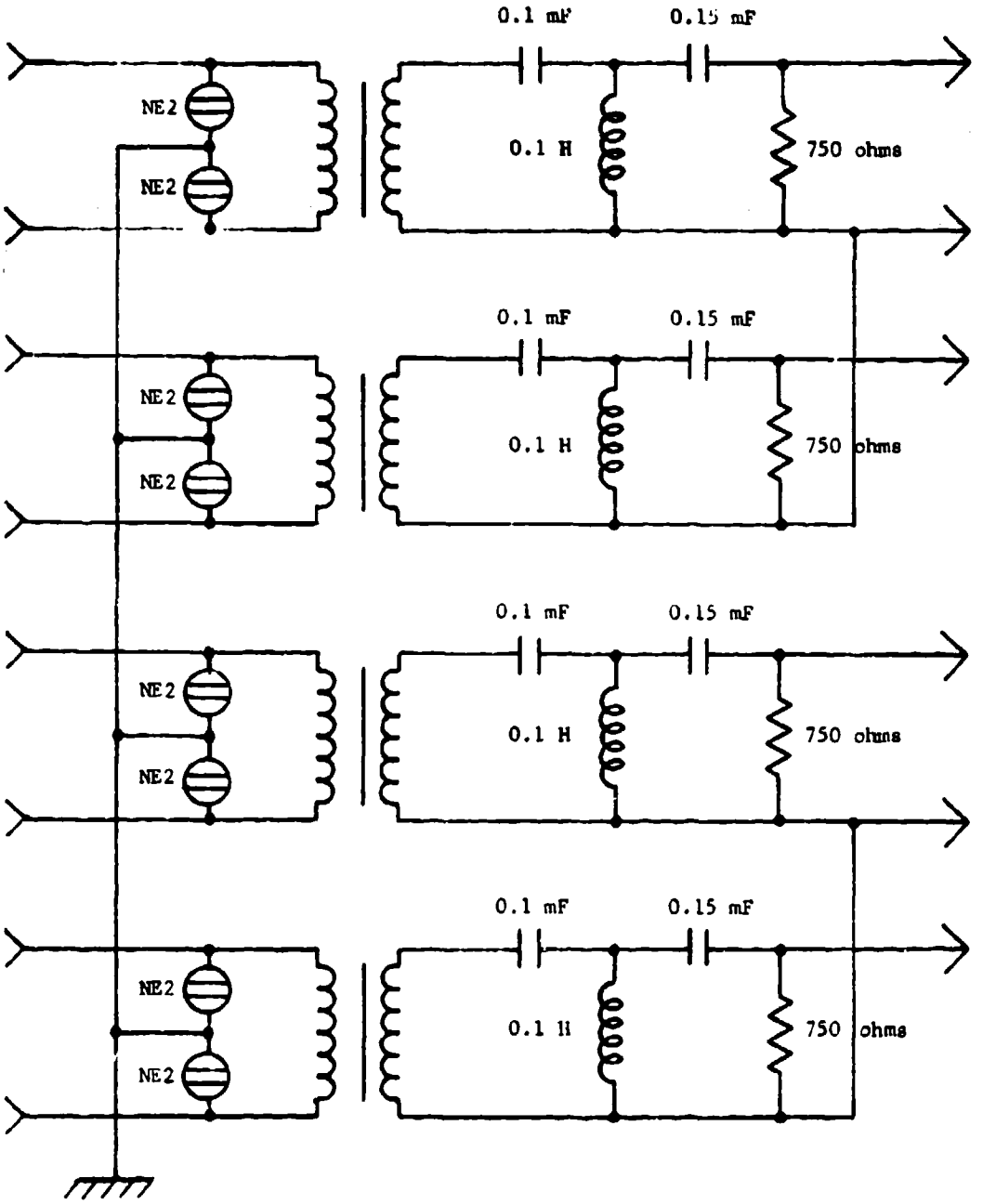


FIGURE 3-30. SCHEMATIC DIAGRAM, BASIC ISOLATION MODULE CIRCUIT

CONFIGURATION CONTROL (Concl'd)

Bit	Purpose
3	FREQUENCY 2 ENABLE 0 = OFF 1 = ON (ENABLED)
2	FREQUENCY 1 ENABLE 0 = OFF 1 = ON (ENABLED)
1	PLAYBACK ENABLE 0 = REAL TIME 1 = PLAYBACK ENABLED
0	SITE SELECTION 0 = ARRAY Y 1 = ARRAY Z.

The configuration control module (CCM) consists of three half-size Cambion circuit boards, two for control of the receivers and one for control of the transmitters.

The two receiver boards are electrically identical, and therefore, interchangeable. They are, however, used to implement slightly different functions when installed in the CCM. Figures 3-31/3-32 show the circuit logic and rel y tree diagram for Receivers 1 and 2, respectively. The relays are Potter and Brumfield fourteen-pin, four-pole, double-throw (DT) relays and, in pairs, allow four channels to be switched betwe.. array Y or array Z in real time, or into playback as shown for beams 1-4 of receiver 1 in Figure 3-31. Two more such pairs are required for beams 5-12 in receiver 1 and the second set of three pairs on the other CCM (receiver 2) are required for the same switching functions for receiver 2.

In unenergized position the module connects each beam of array Y through to its appropriate channel in the analog signal processing boards. To switch to array Z, relays K3, K5, and K7 (on CCM RCVR-1) and relays K9, K11, and K13 (on CCM RCVR-2) must be pulled in. These switching relays are themselves controlled by relay driver Z1 which drives relay K1 on CCM RCVR-1. Relay K1, in turn, switches the energizing current to the site select relays listed above.

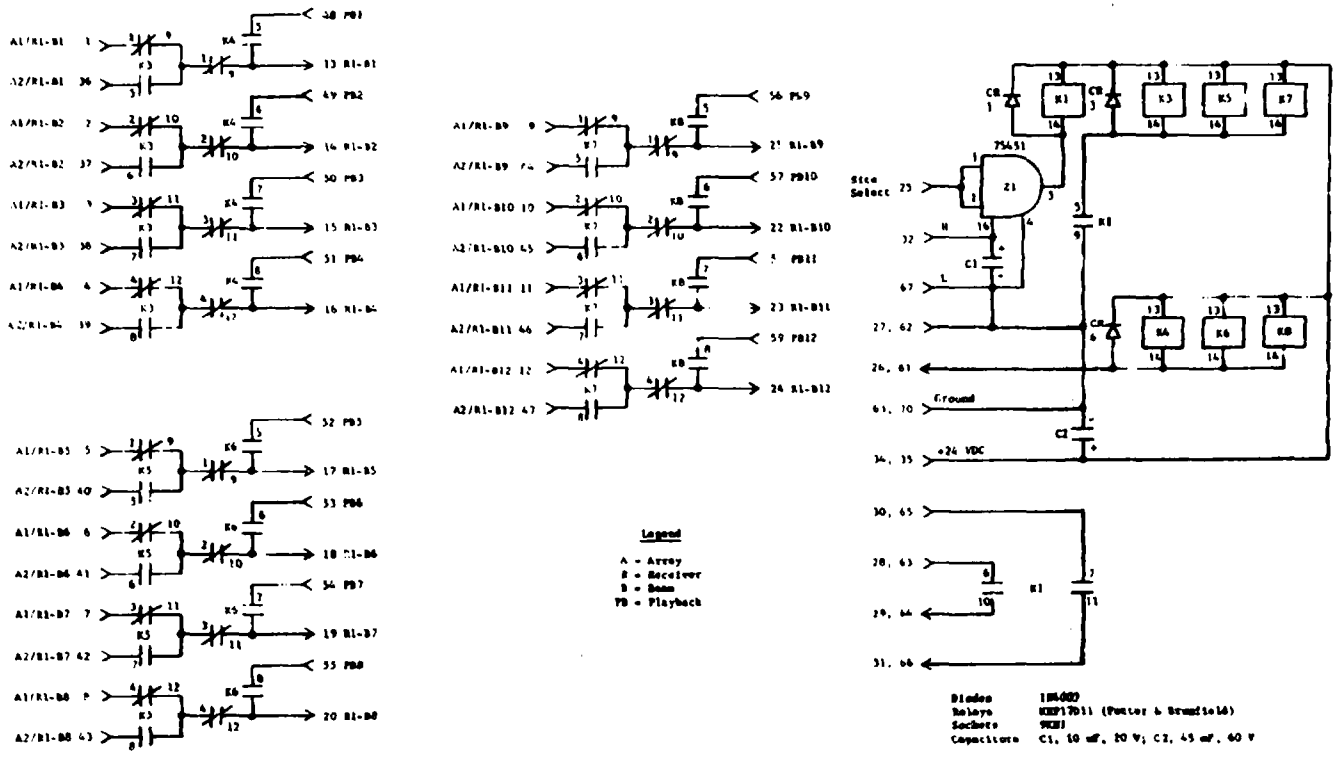


FIGURE 3-31. SCHEMATIC DIAGRAM, CONFIGURATION CONTROL MODULE (RECEIVER 1)

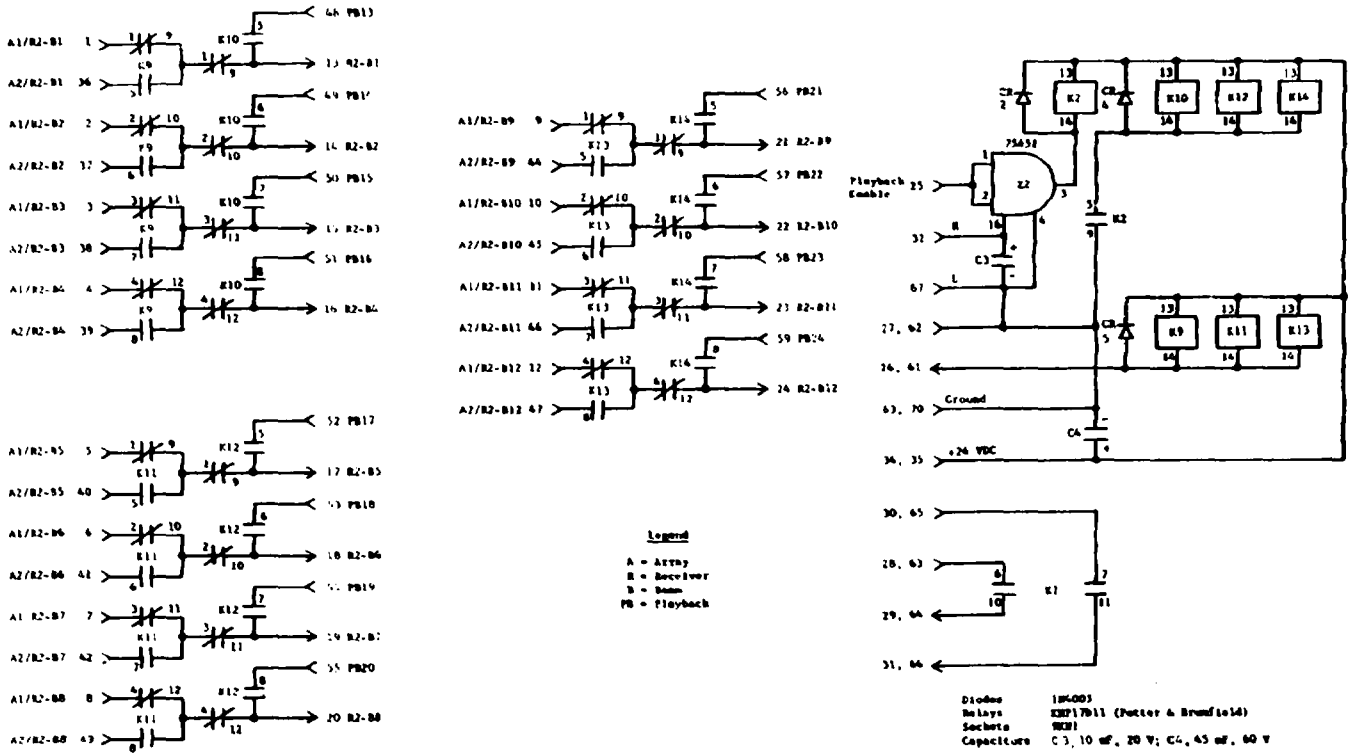


FIGURE 3-32. SCHEMATIC DIAGRAM, *CONFIGURATION CONTROL MODULE (RECEIVER 2)*

To switch the configuration into the playback mode, relays K4, K6, and K8 (on CCM RCVR-1) and relays K10, K12, and K14 (on CCM RCVR-2) must be pulled in. This is accomplished by supplying a logic 1 bit to relay driver Z2 which, in turn, controls relay K2 on CCM RCVR-2. This relay, in turn, pulls in the playback enable switching relays noted above.

The received data is recorded after the first stage of analog signal processing (which is the gain ramp). On playback, the recorded signal is reinserted in the same signal path as the real time signal processor. A playback signal goes through the gain ramp twice; thus on playback the slope should be set to zero.

The configuration control module performs the following three functions for transmitted signals: (1) it allows selection of the array used for transmitting (array Y or Z); (2) it allows selection of the frequencies to be transmitted by XMTR-1 and XMTR-2; and (3) it allows the transmitters to be turned on and off.

The control bit which selects array Y or Z energizes the relay K1 on CCM (RCVR-1). This relay, in turn, controls relay K15 on CCM (XMTRS) and switches the transmitter exciter signals between array Y (unenergized) and array Z (energized), as shown in Figure 3-33. These signals then go through the isolation module and out on their respective cables to the Phase Linear 400 amplifiers at the transmitting antenna assemblies.

The scheme used for frequency selection between XMTR-1 and XMTR-2 through the configuration control module allows the DAVSS to be rapidly switched between the backscatter, pulsed forward scatter, and cw forward scatter modes of operation.

Since all the angle, time delay, and spectral information is derived at the receivers and since there are two sets of receiver channels, it was decided to maintain a constant relationship between the receiving antenna assembly (RCVR-1), analog signal processor boards 1-12, and frequency F1 on the one hand, and between receiving antenna assembly (RCVR-2), analog signal processor boards 13-24, and frequency F2 on the other. The only switching is between array Y and array Z. Consequently, in order to control which transmitter is transmitting to which receiver, the receivers are tuned to the frequency desired by selecting F1 and/or F2. These frequencies are then routed to the transmitter or transmitters required for the mode of operation selected via the switching matrix in CCM (XMTRS). This switching is accomplished through two 4-pole, double throw (4P DT) relays - K18 and K19. The conventional siting of the transmitter and receivers is

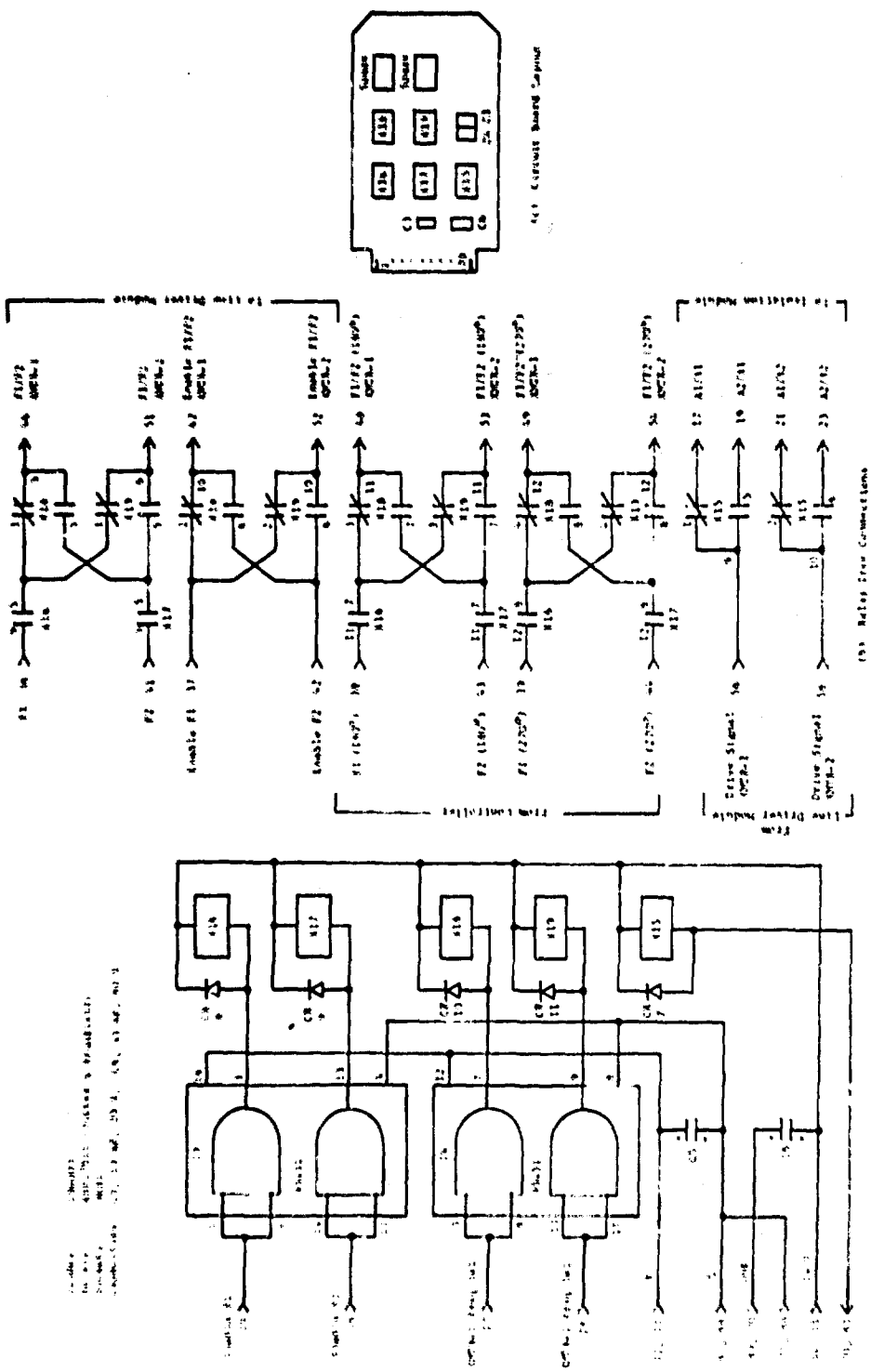


FIGURE 3-33. SCHEMATIC DIAGRAM, CONFIGURATION CONTROL MODULE (TRANSMITTERS)

for XMTR-1 and RCVR-1 and for XMTR-2 and RCVR-2 to be quasi-monostatically located, respectively, as shown in Figure 3-34. Hence, if neither of the relays K18 or K19 is energized, both transmitters will transmit frequency F1. In order to tune RCVR-2 to the proper frequency, F1 and F2 are selected to be the same. Thus, both forward and backscattered signals will be received at each receiver. If K19 is energized and K18 is not, XMTR-1 will transmit F1 and XMTTR-2 will transmit F2; thus if F1 and F2 are signifcantly different, only back scattered signals will be received at each receiver. If K18 is energized and K19 is not, XMTR-1 will transmit F2 and XMTR-2 will transmit F1. Thus, only forward scatter signals will be received at each receiver.

Relays K16 and K17 enable frequencies F1 and F2, respectively, to be fed through the switching matrix to the line driver module and eventually over the cables to the transmitting antenna assemblies. Either or both of the transmitters can be turned off by failing to enable K16 or K17. This is desired during playback, between runs, or when only one transmitter is required to be transmitting.

3.2.3 Envelope Modulator

The envelope modulator performs two basic functions in the DAVSS:

1. Provides signal conditioning to the first and second translation oscillator signals for the analog signal processor boards.

2. Provides filtering and shaping for the exciter signals which are fed to the transmitters.

There are two sets of analog signal processor boards. Boards 1 - 12 are used for receiver 1, while boards 13 - 24 are used for receiver 2. Each receiver utilizes two frequency translations in order to accomplish the desired frequency tuning, notch filtering, band passing, and base band translation for comb filtering and detection. Each translator requires all four quadrant phases of the translation frequency square wave signal at ± 6 volts. Thus, sixteen signals are required, as shown below.

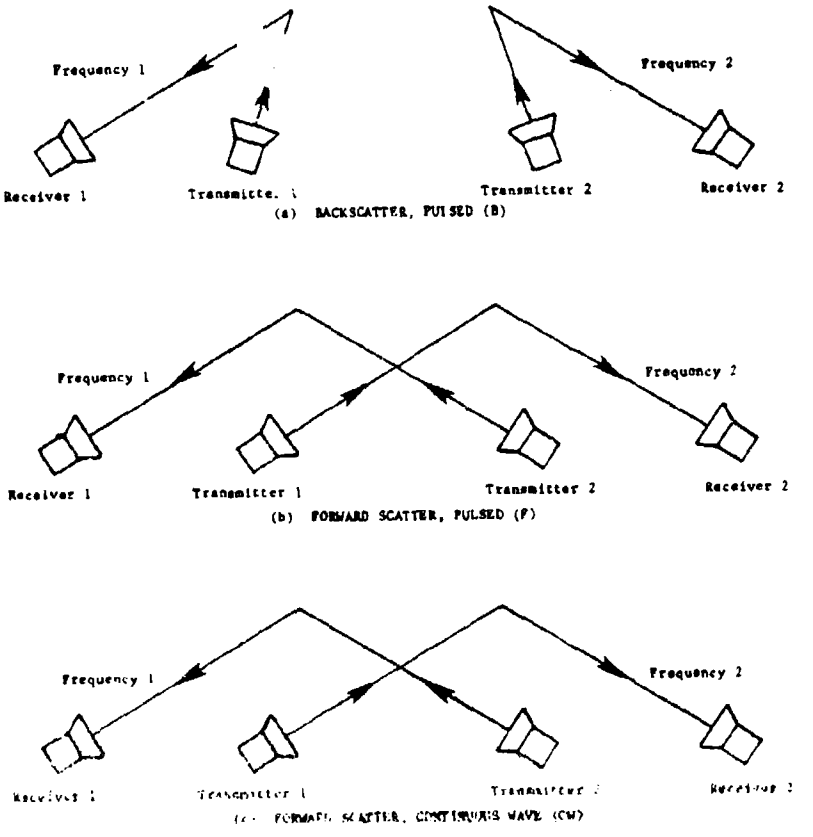


FIGURE 3-34. DOPPLER ACOUSTIC VORTEX SENSING SYSTEM, MODE CONFIGURATIONS

Frequency	Phase	Purpose
F1	0°, 90°, 180°, 270°	1st Translation Oscillator (Receiver 1)
F2	0°, 90°, 180°, 270°	1st Translation Oscillator (Receiver 2)
F3	0°, 90°, 180°, 270°	2nd Translation Oscillator (Receiver 1)
F4	0°, 90°, 180°, 270°	2nd Translation Oscillator (Receiver 2).

Controller board 2 provides the four TTL square wave frequencies required--in-phase and quadrature. The envelope modulator board performs the voltage translation from TTL to ± 6.0 volts and provides an additional 180° phase-shifted signal to each of the 8 signals already supplied, thus producing 0° and 180° phases and 90° and 270° phases as required.

The second function consists of filtering and shaping the pulses prior to feeding them to the line driver module. The line driver module amplifies them to the level required to drive up to 5000 feet of cable and the Phase Linear amplifier at each transmitting antenna assembly. Thus, the signal delivered to the line driver module must be not only of the appropriate carrier frequency but also of the proper pulse shape, length, and reptition period. The basic signal originates as a TTL square wave carrier. (Information to provide the pulse duration and reptition period are derived in controller board 2 from the appropriate clocking signals.) The line driver module input requirement, however, is a sine wave carrier whose pulse shape must be band-limited to approximately 1/T; where T is the pulse duration. Two approaches to achieve this are discussed below.

The first approach is simply to pass the square wave - rectangular envelope pulse through the appropriate bandpass filter. In this case, both the center frequency and the bandwidth of this filter would have to be controlled with roughly the resolution of the carrier frequency and pulse duration; and the bandpass must be multi-pole in order to achieve the desired rejection of the close-in side lobes.

The second approach is to use a low pass filter to convert a square wave carrier into a sine wave, to achieve the desired pulse shaping by low pass filtering the rectangular enevelope of the pulse duration, and to use the resulting output to modulate a voltage controlled amplifier of the carrier signal.

The approach selected is a hybrid of the two. The square wave carrier is first low pass filtered with a constant corner frequency of 5 kHz in order to eliminate the harmonics. The resulting sine wave is multi-

plied by the desired envelope function in a multiplying digital to analog converter (MDAC). The envelope function is designed to approximate a Gaussian pulse shape by using a combination of a sine of an exponential function. The exponential portion of the function is approximated by providing a counter whose count rate is constant within each amplitude octave but doubles for each successive octave so that the counting time for each octave is the same. This running exponential count is fed as the normalized argument to a programmed sine function read-only-memory. The sine function output is then entered as the digital voltage level by which the carrier signal will be multiplied in the MDAC.

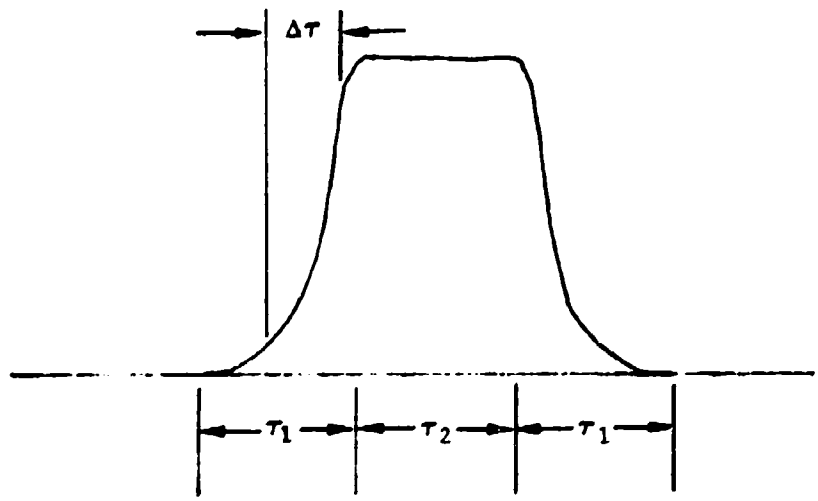
The pulse shape is defined by two parameters: the delay time and the dwell time. The delay time controls the period required to go from the start of the pulse to the maximum amplitude. The dwell time is the duration of the maximum amplitude before the counter is reversed and the amplitude begins to fall as shown in Figure 3-35. The delay time can be controlled in 10 millisecond steps from 10 to 160 milliseconds. The dwell time can be controlled in half millisecond steps from 0-128 milliseconds. Rise time is related to dwell time and is usually defined as the time to go from 10% to 90% of peak amplitude. Because of the complex pulse shape the rise time is considerably shorter than 80% of the delay time.

Figure 3-36 shows the shaped pulse output of the envelope modulator as well as the frequency spectrum of this pulse. These are compared with the shape and spectrum of a rectangular pulse of similar duration.

For operation of the DAVSS in its pulsed Dopper mode it is desireable to maintain as narrow a frequency bandwidth as time resolution requirements on pulse duration will allow. Consequently this somewhat elaborate pulse shaping network which meets those requirements while retaining complete flexibility in the choice of carrier frequency as well as a wide choice of pulse durations and rise times is deemed appropriate.

3.2.4 Line Driver Module

The line driver module is a dual channel power amplifier. It amplifies the outputs of the envelope modulator module and provides impedance matching with the long cable by which the transmitted signals are delivered to the Phase Linear 400 amplifier at each of the transmitting antenna assemblies.



τ_1 = Delay Time

τ_2 = Dwell Time

$\Delta\tau$ = Rise Time (10% - 90%)

FIGURE 3-35. DEFINITION OF PULSE SHAPE OF THE ENVELOPE MODULATOR

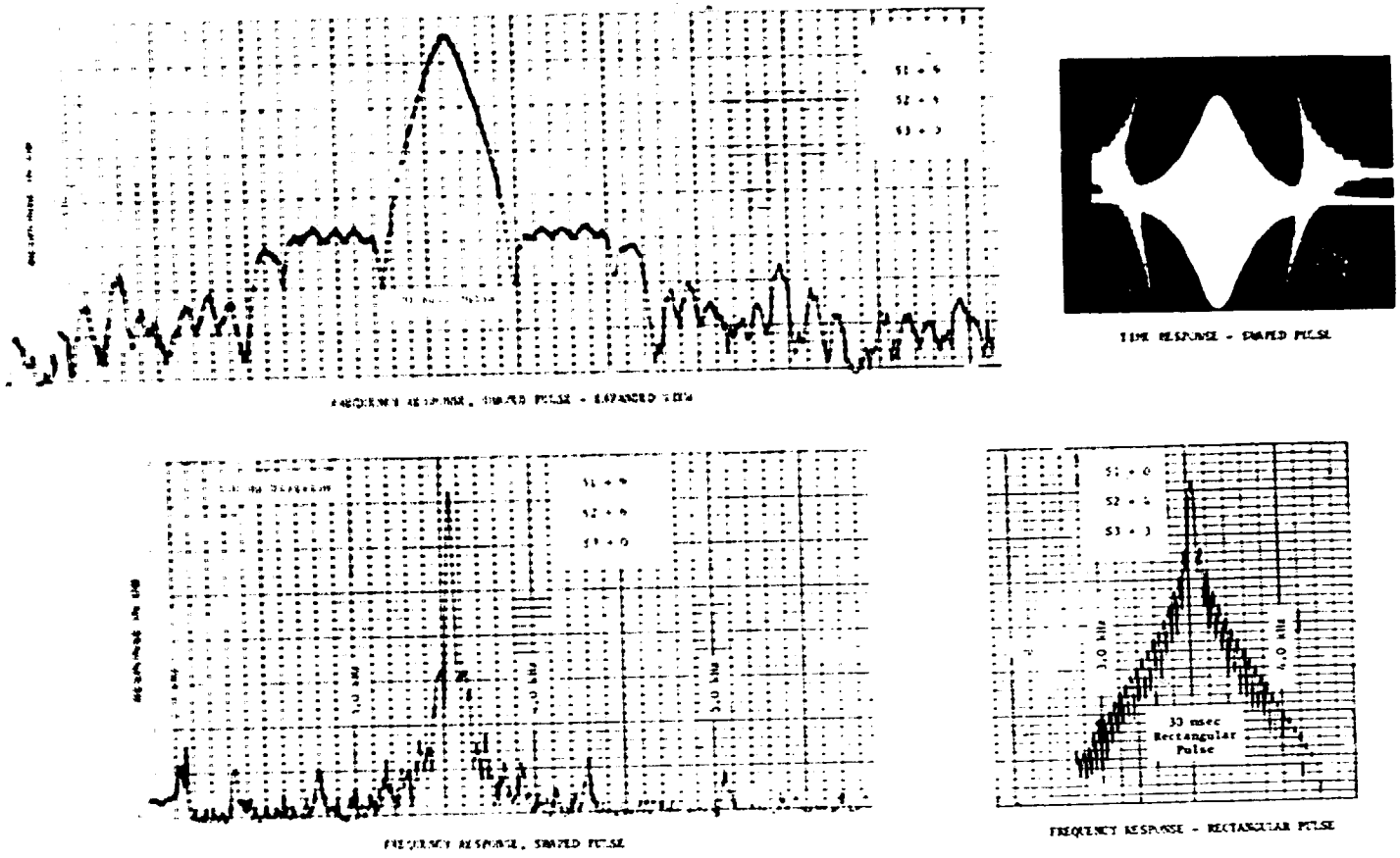


FIGURE 3-36. FREQUENCY AND TIME SPECTRUM OUTPUT OF THE ENVELOPE MODULATOR

Figure 3-37 shows a schematic of the line driver module. The line driver module also contains the 6 volt supplies for the envelope modulator and for radar controller boards 5 and 6. These voltages are used in boards 5 and 6 to convert the transistor-transistor logic (TTL) control bits to ± 6 volts as required to control the selectable parameters of the analog signal processor boards.

3.2.5 Analog Signal Processor

The DAVSS requires twenty-four (24) identical analog signal processing channels. Each of these channels resides on its own analog signal processing board. Boards 1 through 12 are connected to receiver station number 1, and boards 13 - 24 are connected to receiver station number 2 through the configuration control module. Each analog signal processor channel is connected to its own microphone and receiver preamp and monitors the acoustic signal in one beam of the receiving antenna assembly. Within the processor board the individual signal is bandpassed, gain ramped, amplified, notch filtered, and spectrally separated by a six-toothed comb filter and detector. Figure 3-38 is a schematic block diagram of an analog signal processor channel. The controllable parameters are the gain ramp, the first and second translation oscillator frequencies, the translator gain, the notch width, the frequency and bandwidth of the six comb filters, and the detector time constant. The selectable parameters of analog signal processor boards 1 through 12 (station 1) are controlled in parallel; and the parallel control of the selectable parameters of analog signal processor boards 13 through 24 (station 2) is independent of the station 1 boards. Reference to Figure 3-29 shows that the control signals are passed through controller board number 5 in the case of station 1 and through controller board number 6 in the case of station 2. The translation oscillator signals, actually 8 squarewave frequency signals, are provided by the radar controller and envelope module.

The input to the analog signal processor board is from the configuration control module and its first stage is a differential amplifier used to provide additional isolation of each module while increasing the signal level after the long run from the receiver station. The second stage contains the multiplying digital-to-analog converter (MDAC). This

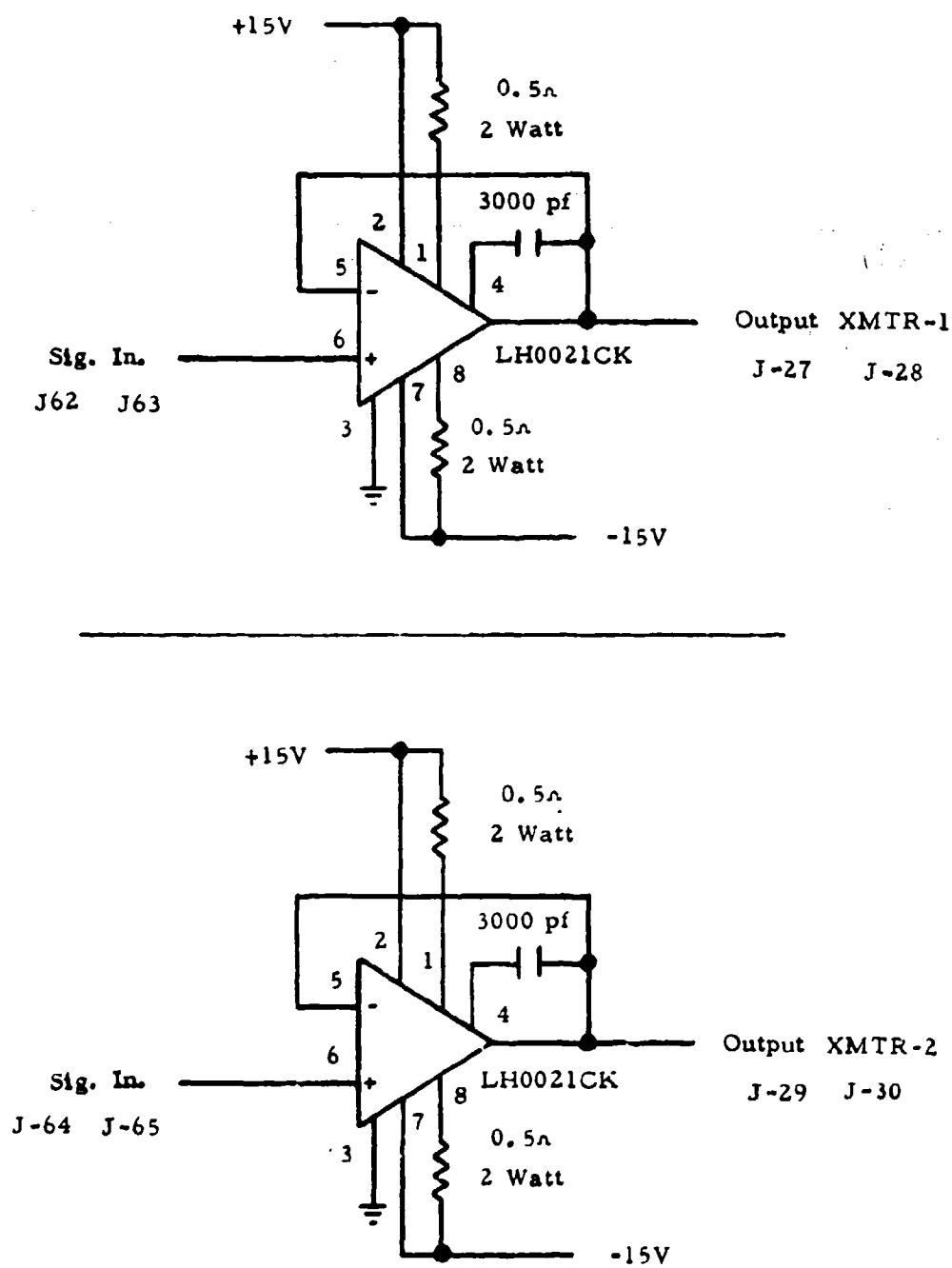


FIGURE 3-37. SCHEMATIC DIAGRAM, LINE DRIVER MODULE

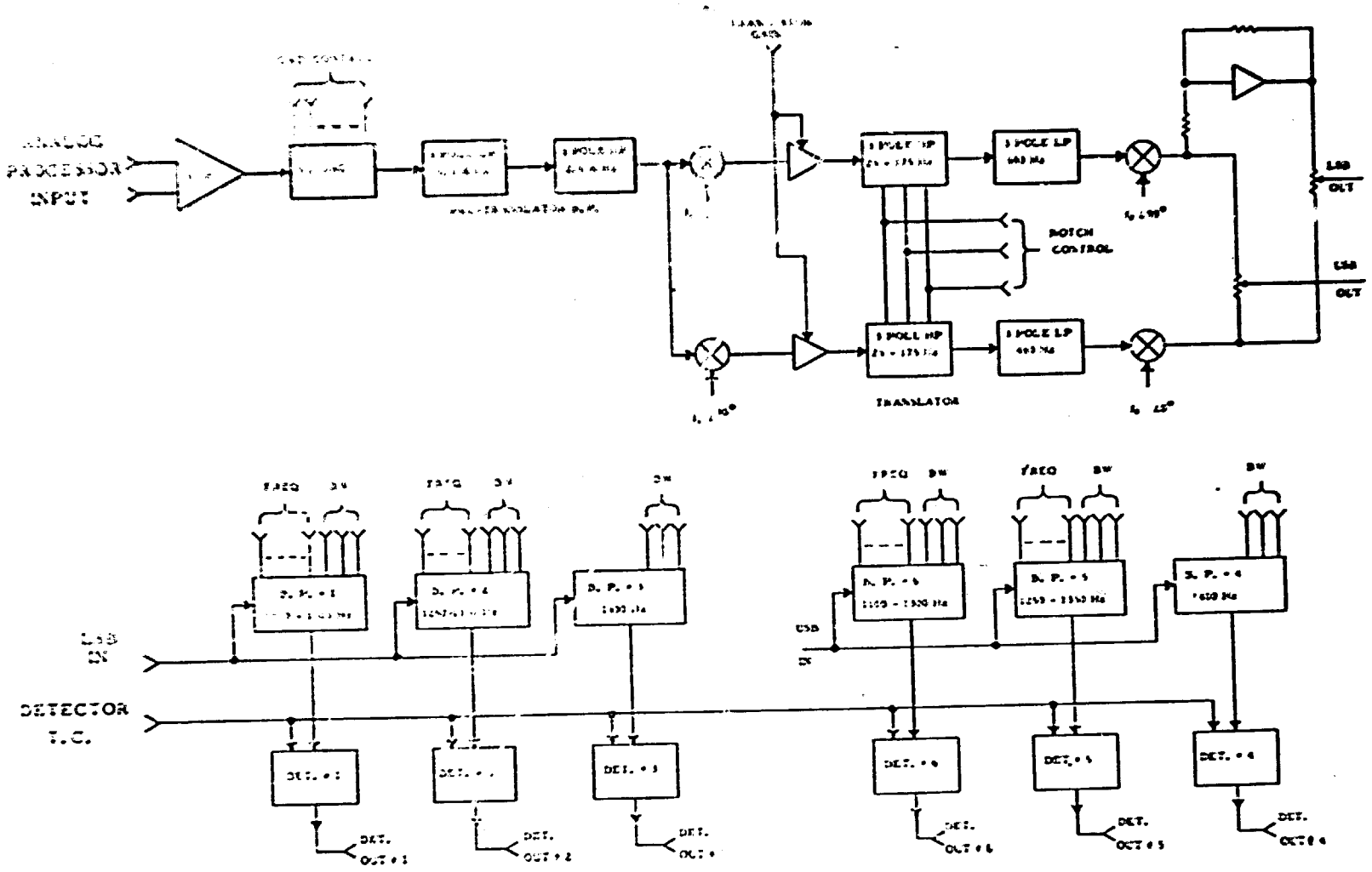


FIGURE 3-38. SCHEMATIC BLOCK DIAGRAM, ANALOG SIGNAL PROCESSOR

stage is used to provide a programmable gain function in order to compensate for the $1/R^2$ loss for target echos at increasing range. The MDAC has two input ports and one output. One input is the signal, the other is a 10-bit parallel input digital count. This count is converted by the D/A converter portion of the MDAC into a voltage which is multiplied by the input signal. The result is an output signal whose gain over the input signal is controlled by the magnitude of the digital count; for the purpose of providing a gain ramp the digital count is independently programmed in controller board 5 for station 1 and in controller board 6 for station 2 to form each linear ramp as shown in Figure 3-39. Four parameters control the ramp gain function: ramp delay, ramp slope, ramp minimum gain, and ramp maximum gain. The minimum gain is the value of the count set in at the beginning of the frame period. This count remains for the duration of the ramp delay. Then the count is incremented with the ramp slope (number of milliseconds per count) until the ramp maximum gain is reached, where upon the incrementing stops and the count remains until the end of the frame. The count is reset at the beginning of each frame to minimum gain.

The next stage of the analog signal processor consists of a three-pole low pass filter with a cut-off frequency of 6 kHz, followed by a three pole high pass filter whose corner frequency is 2.5 kHz. Together these form a bandpass from 2.6 to 6.0 kHz. The purpose of the bandpass is to reject frequencies outside the frequency range of operation of the DAVSS and to insure the rejection of possible image frequencies of the translator network which follows it.

The next stage, the translator network, performs 5 functions: (1) it provides a notch filter to the carrier frequency; (2) it further band limits the processed signal to within ± 500 Hz of the carrier; (3) it translates the processed spectrum to the desired frequency for input to the six comb filters; (4) it inverts the natural upper side band and makes it lower side band so that the filtering action on both the upper and lower side bands is perfectly symmetrical; and (5) it allows for selection of two translator gains to compensate for the signal level difference between the cw and pulsed modes of operation.

The translation is done in-phase and quadrature in two stages. The first stage performs translation to base band. Two signal channels are formed: the in-phase channel and the quadrature channel. Each of the two mixers is a FET mixer and utilizes two square waves 180° out of phase with each other. The in-phase channel uses 0° and 180° phase

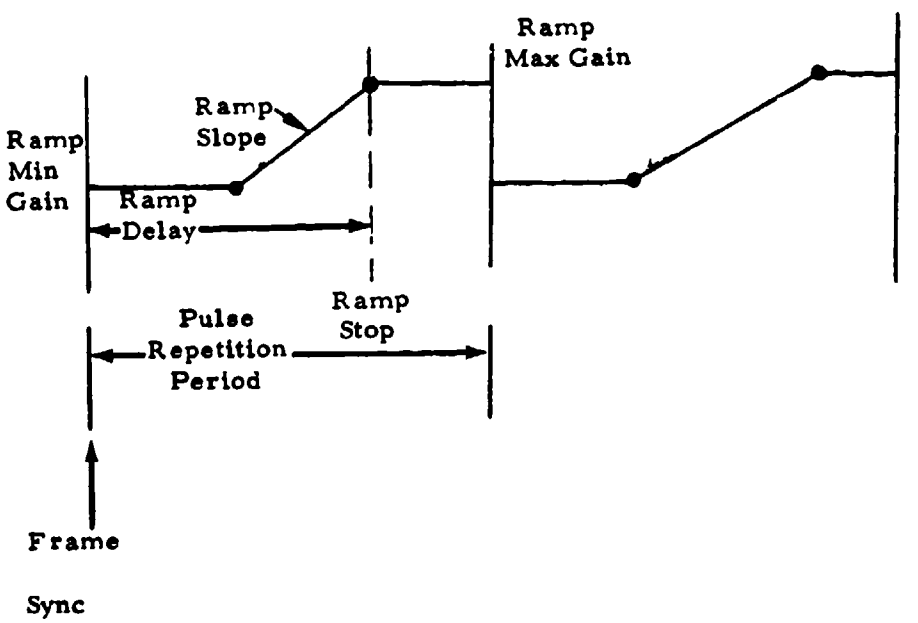


FIGURE 3-39. SCHEMATIC DIAGRAM, LINEAR GAIN RAMP

square waves at the carrier frequency while the quadrature channel uses 90° and 270° phase square waves at the carrier frequency. This dual channel stage translates the initial spectrum down to base band where a three-pole high pass filter effectively notches out the carrier frequency. The high pass cut-off frequency of this filter can be controlled in 25 Hz increments from 25 - 175 Hz. Notch widths from 50 Hz to 350 Hz, selectable in 50-Hz increments result. The high pass in each channel is followed by a three-pole, low pass filter whose corner frequency is 480 Hz. In each channel (in phase and quadrature) this network is followed by a mixer which translates the spectrum back up to a 1500 Hz (nominal) second carrier frequency. The second carrier frequency can be varied from 1400 Hz to 1700 Hz. The variation is used as part of the method of comb filter frequency selection. The mixing and summing of the two in phase and quadrature channels produces two partial spectra. The first represents the lower side band information (-500 Hz to 0) about the transmitted frequency and the second represents the upper side band information (0 to 500 Hz). The upper side band information, however, is inverted and becomes the mirror image of itself about the carrier. Thus, the lower side band information is separated from the upper side band information and both are presented in the bandwidth 1000 Hz to 1500 Hz.

The six comb filters are selectable in the pairs: 1 and 6, 2 and 5, and 3 and 4. They represent the outer, middle, and center-most filters for the lower and upper side band respectively. As shown in Figure 3-38, filters 3 and 4 are fixed at 1400 Hz. Positioning of these center filters for the lower and upper side bands is accomplished by selection of the second translation oscillator frequency in the range 1400 Hz to 1700 Hz. This produces a range of displacement of these filters' center frequency from 0 Hz to 300 Hz. Filters 2 and 5 have a selection range of 1250 - 1350 Hz. This combined with the second translation oscillator range of 1400 Hz - 1700 Hz gives a possible filter displacement from the carrier frequency of 50 Hz - 450 Hz. Filters 1 and 6 have a selection range of 1100 - 1300 Hz which when combined with the second translation oscillator range produces a range of displacements from 200 Hz to 600 Hz. The software is designed to interpret the displacement from the carrier of the center, middle and outer filters desired by the operator into the correct combination of second translation oscillator frequency and individual filter frequencies. Invalid selections are flagged on the GT-40 operator display and must be corrected before the DAVSS operating system will continue.

Each of the filters is followed by its own detector having two selectable time constants. The short time constant (< 10 ms) is selected for pulse mode operation in order to follow the range/time delay variation of the echo signals. The long time constant is selected for cw mode operation in order to maximize the effect of post detection integration.

Each analog signal processor board has six output lines. For receiver 1 these are fed to controller board 5 while for receiver 2 they are fed to controller board 6.

3.2.6 Radar Controller Boards 4, 5, and 6 (Multiplexer, Data Compressor, and Analog/Digital Converter)

Each of the analog signal processor channels produces detected outputs from a comb of six filters. The 24 signal processing channels result in 144 signal lines which must be multiplexed and their outputs converted from analog to digital form for mini-computer processing. This processing requires algorithms to generate three disciminant representations of the set of signals in the six filters for each beam.

Projecting this processing into the time domain by the requirement to preserve the time delay information for pulse mode operations the computational load approaches the limits of the mini-computer's capacity. Therefore, provision was made to implement the three algorithms (intensity, skew, and spread) in analog hardware prior to mini-computer processing.

This analog discriminant processing is done after multiplexing the 144 channels into six serial channels, corresponding to the samples of filters 1 through 6 respectively, in each of the 24 analog signal processors. Since the samples of the six filter outputs of each receiver beam are transformed to samples of the three algorithm values for each beam, a two-to-one compression of data is achieved and the mini-computer is relieved of the burden of computing the algorithms.

Finally, the multiplexer and data compressor output is converted from analog-to-digital form for transfer by "direct memory address" (DMA) to the mini-computer's core memory. Use of the DMA transfer mode eliminates the necessity to generate an interrupt for the transfer of each data word. One interrupt occurs when the whole DMA transfer is complete.

This multiplexer, data compressor, and A/D converter subsystem is situated on three radar controller boards which are designated RCB 4, 5, and 6. Radar controller board 5 is located in the same cage with the receiver 1 processor boards and provides the multiplexing for analog signal processor boards 1 through 12. RCB 6 is located in the same cage with the receiver 2 processor boards and provides multiplexing for analog signal processor boards 13 through 24.

Another stage of multiplexing, data compression and A/D conversion, is accomplished on RCB 4 which is located in the third cage of the data acquisition subsystem. (The rack layout is shown in Figure 3-40) The schematic diagram of the multiplexing scheme is shown in Figure 3-41.

Radar controller boards 5 and 6 are identical. Each provides the following functions:

1. Digital ramp signal for the gain ramps in each of the analog signal processor boards.

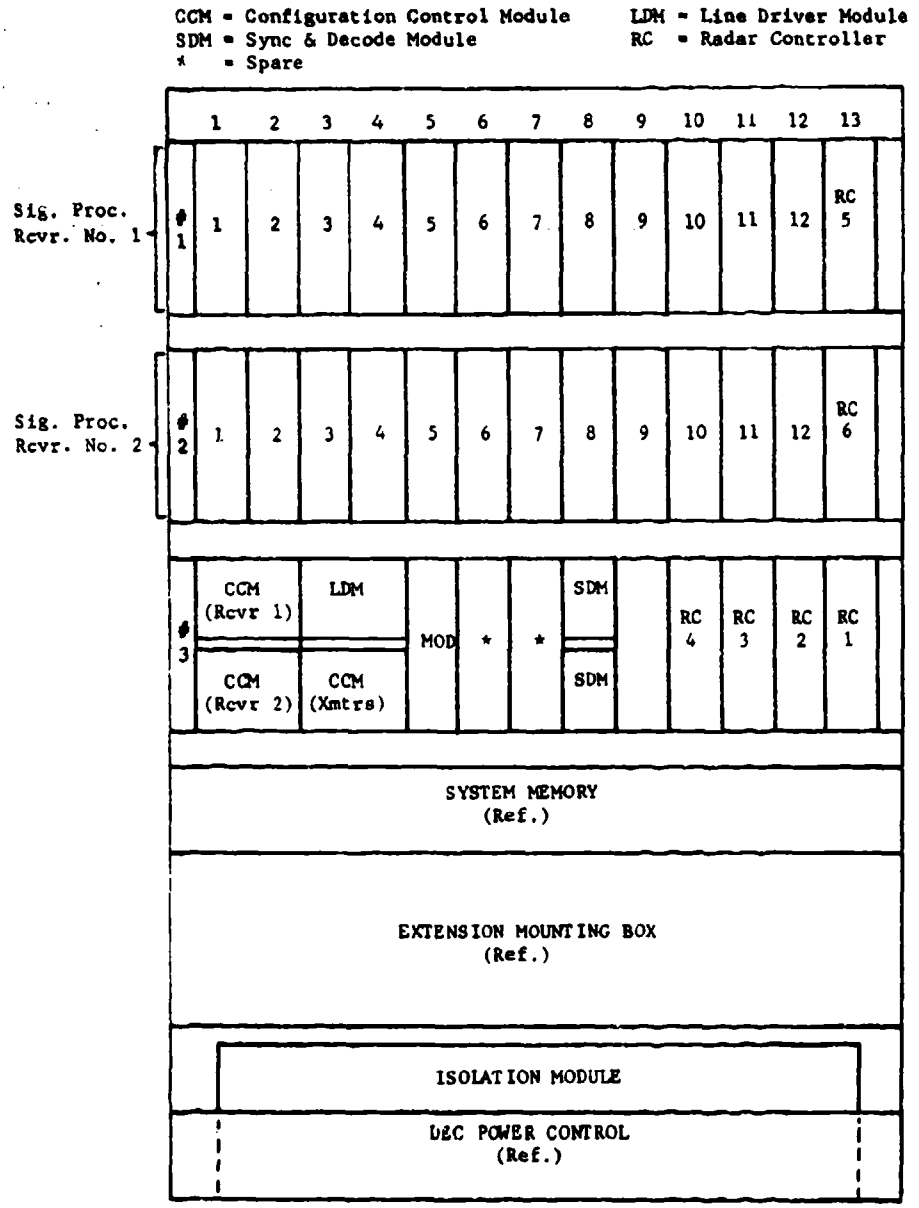
2. Control words for the selectable parameters of the analog signal processor boards.

3. Six 12 to 1 multiplexer channels.

which are discussed below:

1. Digital Ramp

The function of the digital ramp is described in Section 3.2.5 as part of the discussion of the analog signal processor boards. The bit assignment for the specification of the digital ramp is given in Figure 3-42. The two inflection points of the ramp are specified by the operator as the total time delay from the beginning of the frame and as the percentage of maximum gain of the beginning and end of the ramp. The computer uses these values to compute the slope of the ramp. Then, knowing the start point, the value of the end point, and the slope of the ramp, all parameters are defined. The method of providing the ramp of variable slope is to have one counter increment a second counter. The second counter provides the value of the ramp at any time. The first counter provides the variable slope by varying the rate at which the second counter steps. N is the number of counts per second before the counter increments by 1.



NOTES:
1. This is a rear view of the rack.
2. Power supplies are mounted on plates behind front panels.
3. Card file I/O connections: J - top connector; H - bottom connector. Example: 3H11-70 defines pin 70 of bottom connector in slot 11 of card file #3.

FIGURE 3-40. RACK LAYOUT, DATA ACQUISITION SUBSYSTEM

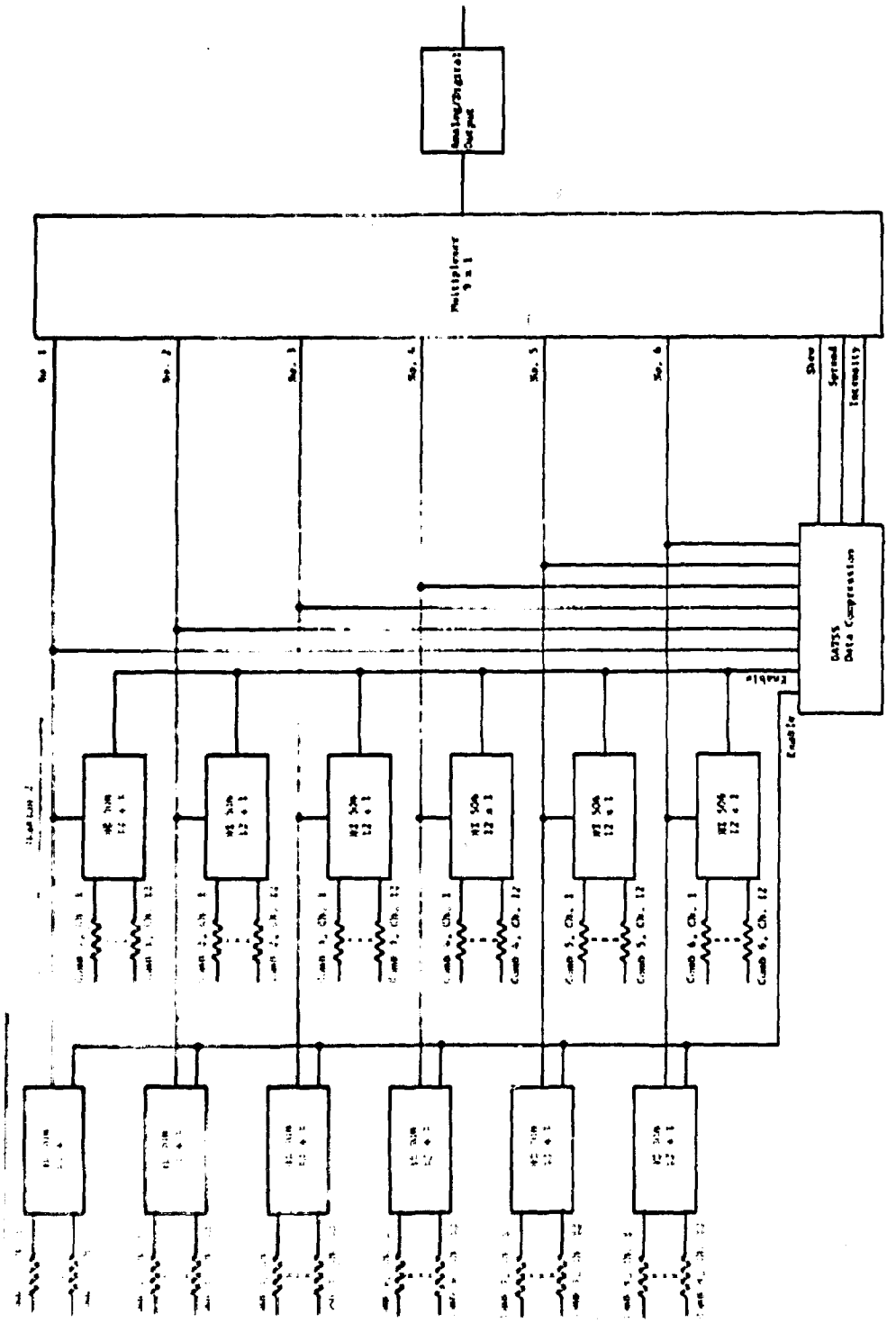


FIGURE 3-41. SCHEMATIC REPRESENTATION OF DAS DATA MULTIPLEXING SCHEME

164112 - RMING 1

RAMP MINIMUM GAIN, STATION 1

Bit	Purpose
15 - 10	Not Used
9 - 0	Ramp Minimum Gain
	0000_8 = 0% 1777_8 = 100%

164114 - RMAXG 1

RAMP MAXIMUM GAIN, STATION 1

Bit	Purpose
15 - 10	Not Used
9 - 0	Ramp Maximum Gain
	0000_8 = 0% 1777_8 = 100%

164106 - RDLY 1

RAMP DELAY, STATION 1

Bit	Purpose	
15 - 8	Not Used	
7 - 0	Ramp Start Delay (msec)	(W)

164110 - RSLOP 1

RAMP SLOPE CONTROL, STATION 1

Bit	Purpose
15 - 12	Not Used
11 - 0	Ramp Slope Control
	N = 12500/Slope (in counts per second)

$$\text{Slope} = \frac{\text{Maximum Counts - Minimum Counts}}{\text{Ramp End Time - Ramp Start Time}}$$

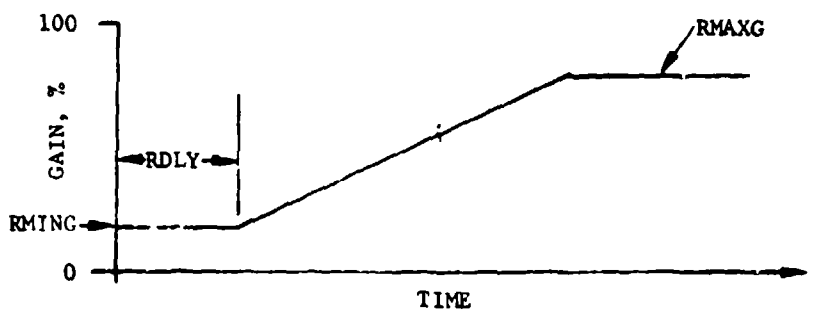


FIGURE 3-42. BIT ASSIGNMENT FOR DIGITAL GAIN RAMP

2. Control Words

Three 16-bit words are used to control the selectable parameters on each set of 12 analog signal processor boards. The bit assignment for each function is shown in Figure 3-43 for station 1 (Rcvr 1). Station 2 (Rcvr 2) is the same except for the word address. The address registers are filled using TTL and so must be converted to ± 6 volts for use on the analog signal processor boards.

3. Multiplexer Channels

The six channels of 12 to 1 multiplexing are composed of six HI506's, one for each filter position as shown in Figure 3-41. The six 12 x 1 multiplexers in station 1 are controlled in parallel so that the six filters are sampled for beam 1, then beam 2, etc. Next, the six filters in station 2 are sampled in parallel for boards 13-24. The sampling address is controlled by a sequencer which is located on radar controller board 4. The operation and capability of this sequencer is outlined as part of the RCB 4 description. The lines for filter 1 are connected in parallel for receiver 1 and receiver 2 so that all twenty-four beam samples for each filter are put onto one line in RCB 4. There are six such lines for the six filters. The multiplexer sampling rate is fast enough to cycle through all 24 beams twice for each time delay resolution period. The clocking rate for the multiplexers is 12.5 kHz so that all of the 24 beams can be sampled in less than 2 msec. This rate is fixed but a second enable bit controls how often a sampling scan is initiated and, therefore, how often each beam is sampled. This beam sampling rate can be fast enought to completely reconstruct any meaningful time delay variation which conveys the range information in the pulsed mode of operation. The sampling rate actually utilized is keyed to the length of transmitter pulse and the range depth desired since there is a storage limit on the total number of samples allowed.

Radar controller board 4 performs the control function for: data selection and scan rates, multiplexing, data compression/algorithm processing, analog-to-digital conversion, and DMA transfer.

164100 - FQBW 121

FREQUENCY & BANDWIDTH - FILTERS 1 & 2, SECTION 1

Bit	Purpose	
15 - 13	Bandwidth Filter 1 (per Graph 1)	(W)
12 - 8	Frequency Filter 1	(W)
	Frequency = 1087.5 + 7.625* N (in Hertz)	
7 - 5	Bandwidth Filter 2 (per Graph 1)	(W)
4 - 0	Frequency Filter 2	(W)
	Frequency = 1142.5 + 6.375* N (in Hertz)	

164102 - FQBW 451

FREQUENCY & BANDWIDTH - FILTERS 4 & 5, SECTION 1

Bit	Purpose	
15 - 13	Bandwidth Filter 4 (per Graph 1)	(W)
12 - 8	Frequency Filter 4	(W)
	Frequency = 1087.5 + 7.625* N (in Hertz)	
7 - 5	Bandwidth Filter 5 (per Graph 1)	(W)
4 - 0	Frequency Filter 5	(W)
	Frequency = 1142.5 + 6.375* N (in Hertz)	

154104 - BW36N1

BANDWIDTH FILTERS 3 & 6, AND NOTCH, STATION 1

Bit	Purpose	
15 - 11	Not Used	
10	Detector Time Constant 0 = Short (Pulsed) 1 = Long (Continuous Wave)	
9	Gain Control 0 = High (Pulsed) 1 = Low (Continuous Wave)	
8 - 6	Notch Bandwidth = 50* N (in Hertz)	(W)
5 - 3	Bandwidth Filter 6 (per Graph 1)	(W)
2 - 0	Bandwidth Filter 3 (per Graph 1)	(W)

FIGURE 3-43. BIT ASSIGNMENT FOR CONTROL OF SELECTABLE PARAMETERS OF ANALOG SIGNAL PROCESSOR BOARDS

Multiplexed data is provided to RCB 4 which contains the six filtered samples from beams 1 - 24 for each scan period. These six lines go to a 9 x 1 multiplexer and to the data compression circuitry.

The outputs of the data compression circuit are three lines which represent the three discriminants - intensity, spread, and skew. The six raw filter outputs and the three discriminant outputs make up the nine lines into the 9 x 1 multiplexer. The 9 x 1 multiplexer is followed by an analog-to-digital converter in which the serial analog multiplexed signals are converted to 8-bit digital words which are then transferred by direct memory address (DMA) to the computer core memory in one block. This DMA transfer block corresonds to all the received and processed data for a single frame; i.e., one pulse reptition period for the pulsed mode or an arbitrary, operator selectable time period for the cw mode.

Figure 3-44 shows the bit assignments for the data selection word on RCB 4. It also shows the various possibilities for data selection. One may make a selection from the following three choices:

1. Constantly monitor any single filter or discriminant in any single beam in either receiver 1 or 2.

2. Scan the discriminants or raw filter data in all beams of receiver 1 or receiver 2 or both.

3. Scan either discriminants or the raw filter data in only the odd-numbered channels or the even-numbered channels of receiver 1 or receiver 2 or both.

164074 - DATSEL

DATA SELECTION

	Bit	Purpose	
A	15 - 12	Filter Number, or Discriminant Selection 0 - 5 = N = Filter Number Selected 6 - 12 = N = Invalid 13 = N = Spread Discriminant Selected 14 = N = Skew Discriminant Selected 15 = N = Intensity Selected	(W)
A	11 - 8	Channel Number 1 Selected N = 11 = Invalid	(W)
A	7	Station 1 Enabled 0 Disabled; 1 = Enabled	(W)
A	6	Station 2 Enabled 0 = Disabled; 1 = Enabled	(W)
B	5	Scan Mode 0 = Scan All Channels 1 = Scan Only Every Other Channel	(W)
B	4	Scan Odd/Even Channels 0 = Scan Odd-Numbered Channels 1 = Scan Even-Numbered Channels (Effective only if Bit 5 = 1)	(W)
B, C	3	Station 2 Discriminants 0 = Do Not Scan 1 = Scan	(W)
B, C	2	Station 1 Discriminants 0 = Do Not Scan 1 = Scan	(W)
B, D	1	Station 2 Raw Data 0 = Do Not Scan 1 = Scan	(W)
B, D	0	Station 1 Raw Data 0 = Do Not Scan 1 = Scan	(W)

Notes:

Bits 6 and 7 must never be set together.
Bit Groups A and B are mutually exclusive. That is, if any bit in Group A is set, then none in Group B may be set, and vice versa.
Bit Groups C and D are likewise mutually exclusive.

FIGURE 3-44. BIT ASSIGNMENT FOR DATA SELECTION WORD

The three discriminants which are formed in the data compression circuits are: intensity, spread, and skew. Each of these three discriminants is designed to combine the outputs of the six comb filters in a manner which emphasizes one of the characteristics of the output spectrum. Intensity, as the name implies, gives an estimate of the average intensity of the spectrum.

Spread is intended to given an estimate of the width of the spectrum; while skew is intended to given an estimate of the first moment of the Doppler spectrum.

Figure 3-45 shows the schematic of the analog data compression circuitry. The intensity discriminant is represented by:

$$\text{Intensity} = \sum_{i=1}^{6} A_i ,$$

where

A_i is the amplitude of data from filter i

i is the designation of the filter line from 1 to 6.

Thus, the amplitudes of all six filters are summed together and the result is scaled by the value of the summing resistor in the amplifying circuit.

Spread and skew utilize symmetric and antisymmetric weighting of the values of the upper and lower side band filters in the summing operation. The weighting is accomplished by using the 8-bit digital weight, K_i as the Y-input multiplier in an MDAC in order to multiply each of the X-input comb filter values X_i . The values of the weights are set into the 16-bit register - K1 through K6- where the first 8 bits correspond to the weights for receiver 1. A 96 x 48 multiplexer switches the appropriate 8 bits into the 8-bit MDAC. The first 8 bits are for use with the data stream coming from receiver 1 and the second 8 bits for the data from receiver 2.

The weighted outputs of filters 1, 2, and 3 are summed in one amplifier and the weighted outputs of filters 4, 5, and 6 are summed in the other.

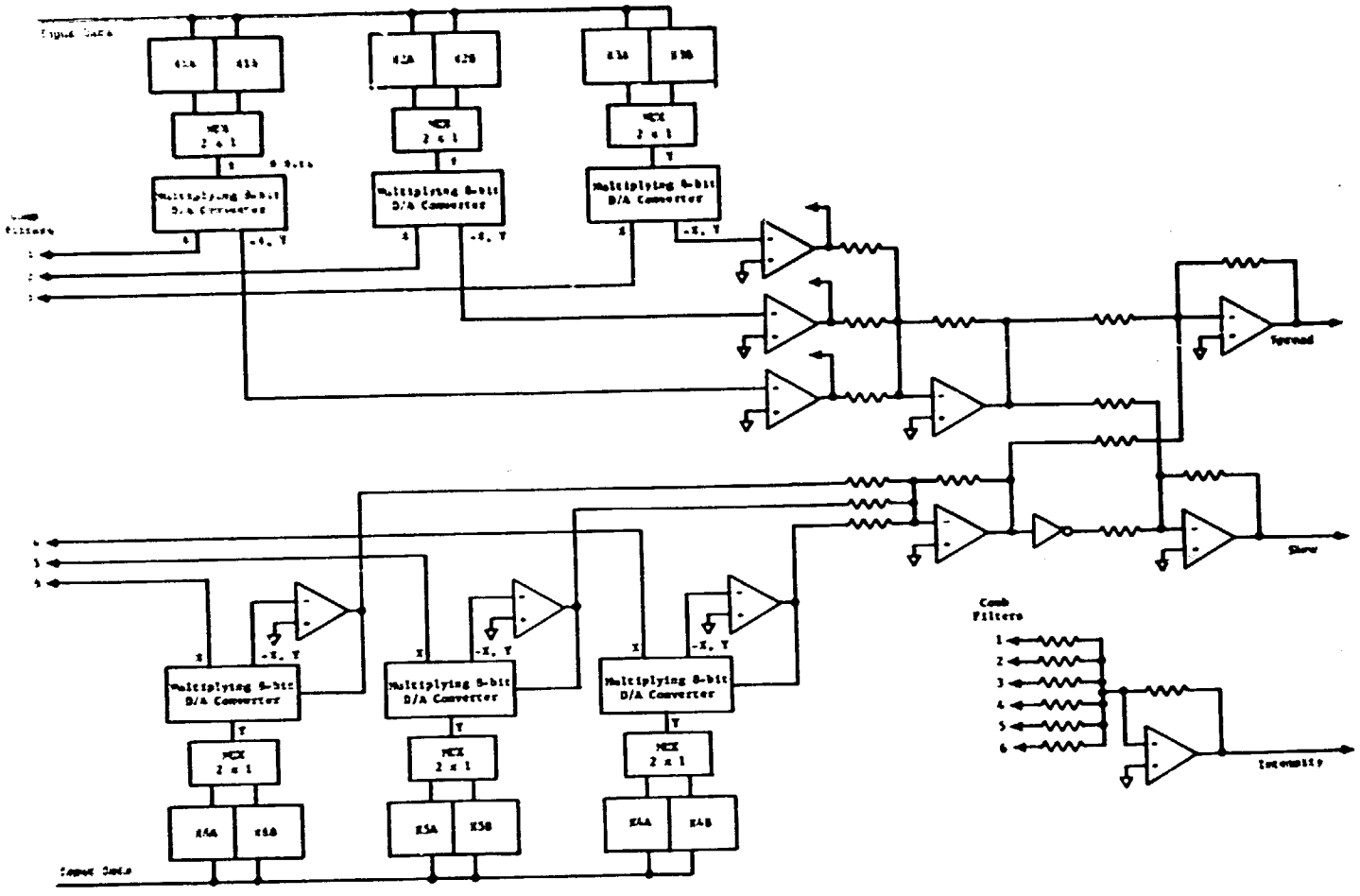


FIGURE 3-45. SCHEMATIC DIAGRAM, ANALOG DATA COMPRESSION CIRCUITRY

The spread discriminant is formed by summing the results of these two.

$$\text{Spread} = \sum_{i=1}^{3} \text{Ki Ai} + \sum_{i=4}^{6} \text{Ki Ai} = \sum_{i=1}^{6} \text{Ki Ai}.$$

Skew, on the other hand, is formed by taking the difference of these same two subtotals:

$$\text{Skew} = \sum_{i=1}^{3} \text{Ki Ai} - \sum_{i=4}^{6} \text{Ki Ai}.$$

In practice, in order to maintain the symmetric/antisymmetric nature of the spread and skew discriminant algorithms, K_1 and K_6, K_2 and K_5, and K_3 and K_4 are chosen to be the same. In addition, they are usually chosen such that

$$K_1 = K_6 \geq K_2 = K_5 \geq K_3 = K_4$$

Figure 3-46 shows the bit assignment of the Ki weights for each of the six filters for both station 1 and station 2.

3.2.7 Radar Controller Boards (RCB 1, 2, and 3)

The radar controller is the heart of the data acquisition subsystem. It regulates all data flow between the radar sites and the central processor. Basically it consists of a set of registers that allow the initial run parameters to be loaded. These parameters include: carrier frequency, pulse characteristics (pulse width and repetition frequency), mode of operation, and data sampling rate. The radar controller also includes a command status register used to accept external commands. In addition to these registers, the controller contains the standard registers and circuitry needed to allow interrupt and direct memory address (DMA) transfers to the computer core memory.

Briefly then, the controller receives all information pertaining to the mode of operation, translates this information into the appropriate control functions, and effects data transfer.

The principal functions of radar controller boards 4, 5 and 6 have been outlined in paragraph 3.2.6 describing the data multiplexing, compression, and analog to digital conversion prior to DMA transfer to the mini-computer. The functions of the remaining radar controller boards 1, 2, and 3 are described in this paragraph. Figure 3-47 shows the

164060 - CFG 1

COMB FILTER GAIN 1, STATIONS 1 & 2

Bits 15 - 8	Comb Filter Number 1, Station 2 - Positive Gain	(W)
Bits 7 - 0	Comb Filter Number 1, Station 1 - Positive Gain	(W)

164062 - CFG 2

COMB FILTER GAIN 2, STATIONS 1 & 2

Bits 15 - 8	Comb Filter Number 2, Station 2 - Positive Gain	(W)
Bits 7 - 0	Comb Filter Number 2, Station 1 - Positive Gain	(W)

164064 - CFG 3

COMB FILTER GAIN 3, STATIONS 1 & 2

Bits 15 - 8	Comb Filter Number 3, Station 2 - Positive Gain	(W)
Bits 7 - 0	Comb Filter Number 3, Station 1 - Positive Gain	(W)

164066 - CFG 4

COMB FILTER GAIN 4, STATIONS 1 & 2

Bits 15 - 8	Comb Filter Number 4, Station 2 - Positive Gain	(W)
Bits 7 - 0	Comb Filter Number 4, Station 1 - Positive Gain	(W)

164070 - CFG 5

COMB FILTER GAIN 5, STATIONS 1 & 2

Bits 15 - 8	Comb Filter Number 5, Station 2 - Positive Gain	(W)
Bits 7 - 0	Comb Filter Number 5, Station 1 - Positive Gain	(W)

164072 - CFG 6

COMB FILTER GAIN 6, STATIONS 1 & 2

Bits 15 - 8	Comb Filter Number 6, Station 2 - Positive Gain	(W)
Bits 7 - 0	Comb Filter Number 6, Station 1 - Positive Gain	(W)

Note: In normal operation:
CFG 1 = CFG 4
CFG 2 = CFG 5
CFG 3 = CFG 6
CFG 4 = CFG 1
CFG 5 = CFG 2
CFG 6 = CFG 3.

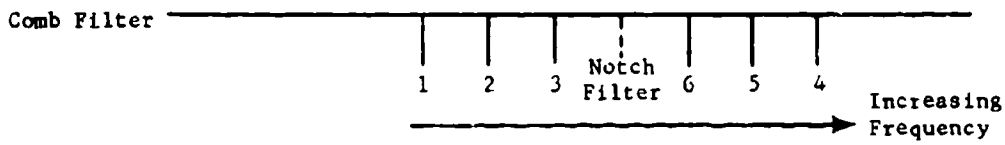


FIGURE 3-46. BIT ASSIGNMENT FOR Ki WEIGHTS FOR THE ANALOG DATA COMPRESSION CIRCUITS

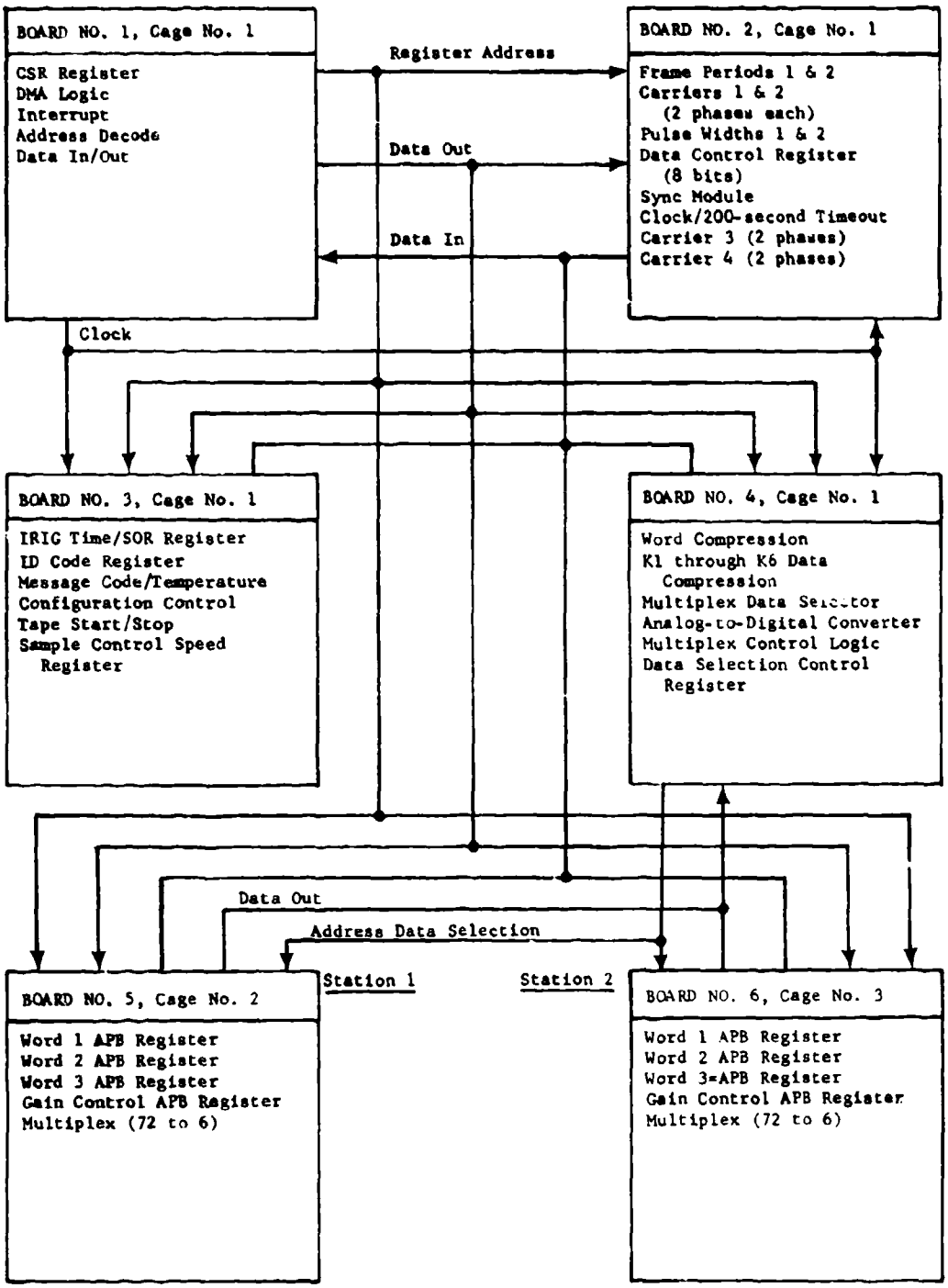


FIGURE 3-47. DAS CONTROLLER CONFIGURATION

board configuration of the DAVSS radar controller and the functions each board performs.

3.2.7.1 Radar Controller Board No. 1 Functions

The logic flow of radar controller board 1 is shown in Figure 3-48.

1. Command Status Register

The command status register (CSR) is a 16-bit read/write register. The lower 8 bits are read/write bits to activate various registers in the controller. The upper 8 bits are read-only bits for indicating the interrupt mode of the system. Bit usage is presented in Figure 3-49. The terms read-only and write-only are from the point of view of the computer. That is, the read-only bits are set by other functions in the controller and are read by the computer. The write-only bits are written by the computer and become enable bits to other control logic in the computer. The 0 bit is an enable bit for the CSR and is logically connected such that neither the read nor the write functions will be operable unless it is set. The upper bits, 8-15 are set by other registers within the controller upon controller issued interrupt to the computer. They tell the computer which kind of controller interrupt was issued and which branch of the operating program to take.

2. Direct Memory Address (DMA)

The direct memory address logic is provided for depositing data from the A/D converter on RCB 4 into memory. The DMA operates on byte addressing with the full 16-bit control register. The DMA gives a done interrupt on completion of the transfer of the data block and also an interrupt for the end of frame interrupt with the address of the last data transfer channel.

3. Interrupt/Address Decode

The interrupt/address decode uses the standard Digital Equipment Corporation interrupt circuitry. The one vector address is selectable via a plug-in component adapter. The basic address of the controller is 764. The address decoder decodes the addresses for use with the controller. The addresses and their functions are listed in Table 3-7.

4. Data Input/Output

The data input from the mini-computer and output to the mini-computer are accomplished through the radar controller board 1.

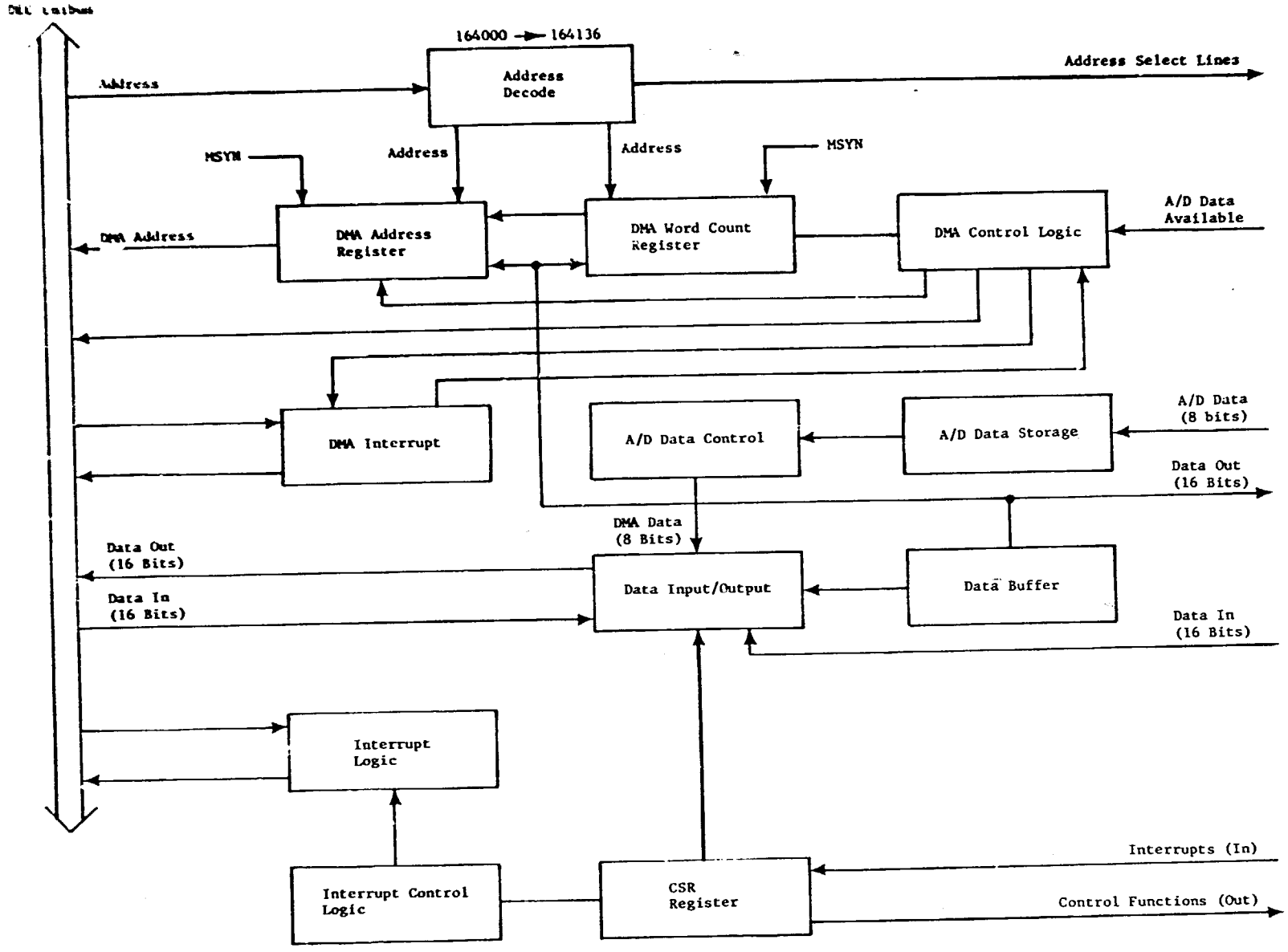


FIGURE 3-48. LOGIC FLOW, RADAR CONTROLLER, BOARD NO. 1

164000 - ACCSR

COMMAND AND STATUS REGISTER

Bit	Purpose	Read	Write
15	Direct Memory Address (DMA) Failure (a programming error)	R	
14	Time - Start of Run (SOR)	R	
13	DMA Complete	R	
12	Not Used	R	
11	External Ready	R	
10	ID Word Ready	R	
9	Run Time Out (200 seconds)	R	
8	Message Call (aircraft type)	R	
7	Done (write ID)	R	
6	Interrupt Enable	R	W
5	DMA Enable	R	W
4	End-of-Frame Interrupt Enable	R	W
3	Not Used		
2	ID Code Enable	R	W
1	Playback Enable	R	W
0	Enable	R	W

FIGURE 3-49. BIT ASSIGNMENT, COMMAND STATUS REGISTER

TABLE 3-7

CONTROLLER ADDRESSES

ADDRESS	SOFTWARE NAME	FUNCTION
164000	ACCSR	COMMAND AND STATUS REGISTER
164002	DMAAD	CURRENT DIRECT MEMORY ACCESS ADDRESS
164004	DMABC	DIRECT MEMORY ACCESS BYTE COUNT
164006	OPSTRT	START 200 SEC TIMER
164010	OPREDY	RESET 200 SEC TIMER
164012	FRAMO	FRAME 2 OFFSET FROM FRAME 1 (OR FRAME 2 PERIOD)
164014	FRAMP	FRAME 1 LENGTH
164016	PW2	PULSE WIDTH 2 (VESTIGIAL)
164020	PW1	PULSE WIDTH 1 (VESTIGIAL)
164022	TFRQ2	TRANSLATION FREQUENCY, STATION 2
164024	TFRQ1	TRANSLATION FREQUENCY, STATION 1
164026	FFRQ2	NOTCH FILTER FREQUENCY, STATION 2
164030	FFRQ1	NOTCH FILTER FREQUENCY, STATION 1
164032	CONFC	CONFIGURATION CONTROL
164034	IDCODE	RUN IDENTIFICATION CODE REGISTER
164036	MSCDAT	A/C MESSAGE (AND TEMPERATURE, NOT IMPLEMENTED)

TABLE 3-7 (CONT'D)

CONTROLLER ADDRESSES

ADDRESS	SOFTWARE NAME	FUNCTION
164040	TAPESS	ANALOG TAPE RECORDER START-STOP
164042	IRIGT	IRIG TIME
164044	PSHAPE1	PULSE SHAPE, STATION 1
164046	PSHAPE2	PULSE SHAPE, STATION 2
164050	DMADLY	DMA INITIATION DELAY FROM FRAME SYNC
164052	DMAPER	DMA DATA SCAN PERIOD
164054	DMACONF	DMA CONFIGURATION
164056	SPARE 1	SPARE
164060	CFG1	COMB FILTER GAIN 1, STATION 1 & 2
164062	CFG2	COMB FILTER GAIN 2, STATION 1 & 2
164064	CFG3	COMB FILTER GAIN 3, STATION 1 & 2
164066	CFG4	COMB FILTER GAIN 4, STATION 1 & 2
164070	CFG5	COMB FILTER GAIN 5, STATION 1 & 2
164072	CFG6	COMB FILTER GAIN 6, STATION 1 & 2
164074	DATSEL	DATA SELECTION
164076	SPARE 2	SPARE
164100	FQBW121	FREQUENCY AND BANDWIDTH- FILTER 1 & 2-STATION 1

TABLE 3-7 (CONCL'D)

CONTROLLER ADDRESSES

ADDRESS	SOFTWARE NAME	FUNCTION
164102	FQBW451	FREQUENCY AND BANDWIDTH-FILTER 4 & 5-STATION 1
164104	BW36N1	BANDWIDTH-FILTER 3 & 6 & NOTCH-STATION 1
164106	RDLY1	RAMP DELAY-STATION 1
164110	RSLOP1	RAMP SLOPE-STATION 1
164112	RMING1	RAMP MIN. GAIN-STATION 1
164114	RMAXG1	RAMP MAX GAIN-STATION 1
164116	SPARE3	SPARE
164120	RQBW122	FREQUENCY AND BANDWIDTH-FILTER 1 & 2-STATION 2
164122	FQBW452	FREQUENCY AND BANDWIDTH-FILTER 4 & 5-STATION 2
164124	BW36N2	BANDWIDTH-FILTER 3 & 6 & NOTCH-STATION 2
164126	RDLY2	RAMP DELAY-STATION 2
164130	RSLOP2	RAMP SLOPE-STATION 2
164132	RMING2	RAMP MIN. GAIN-STATION 2
164134	RMAXG2	RAMP MAX. GAIN-STATION 2

3.2.7.2 Radar Controller Board 2 Functions

The logic flow of RCB 2 is shown in Figure 3-50.

1. Frame Period 1 and 2 Generation

There are two frame period generators, one for each transmitter and receiver pair. Each frameperiod generator is controlled by a 12-bit code set in from the computer. The set in code is compared with a counter and when they match, the frame generator sends out a pulse to activate the pulse width generator and resets the counter for a new cycle. The frame generator is clocked by a 1 kHz signal thus providing 1 millisecond resolution for the frame period. The maximum frame period is 4.095 seconds. Frame period 2 can also be set to a fixed delay from frame 1.

2. Pulse Width 1 and 2 Generator Control

There are two pulse width generators, one for each transmitter and receiver pair in the active array. The pulse width is set by using a 12-bit word. The pulse width generator is clocked by a 1 kHz generator and thus the maximum pulse length is 4, 095 milliseconds. The pulse width generator upon being enabled by the frame generator, sends out an enable pulse to the synchronization module and maintains the enable pulse for the duration of the pulse period.

3. Carrier Frequency 1, 2, 3 and 4 Generator Control

Four frequency generators are required to provide mixing frequencies to the first and second translation oscillators in the analog signal processor boards of receiver 1 and receiver 2. In addition, the first mixing frequency is the carrier frequency for the transmitted signals. Each frequency is generated by a programmable counter controlled by a 12-bit code. The code set in is 4 times the frequency required. The output of the programmable counter is divided by two twice in order to provide the two quadratures. The other two quadratures are added in the envelope modulator in order to provide the four quadratures required by the analog signal processor boards. The frequency range is (5 MHz/4N) where the N range is from 2 to 4, 095. The frequency range, therefore, is from 625 kHz to 305 Hz. The precision is 20-Hz steps at 5000 Hz and less than 5 Hz at 2500 Hz.

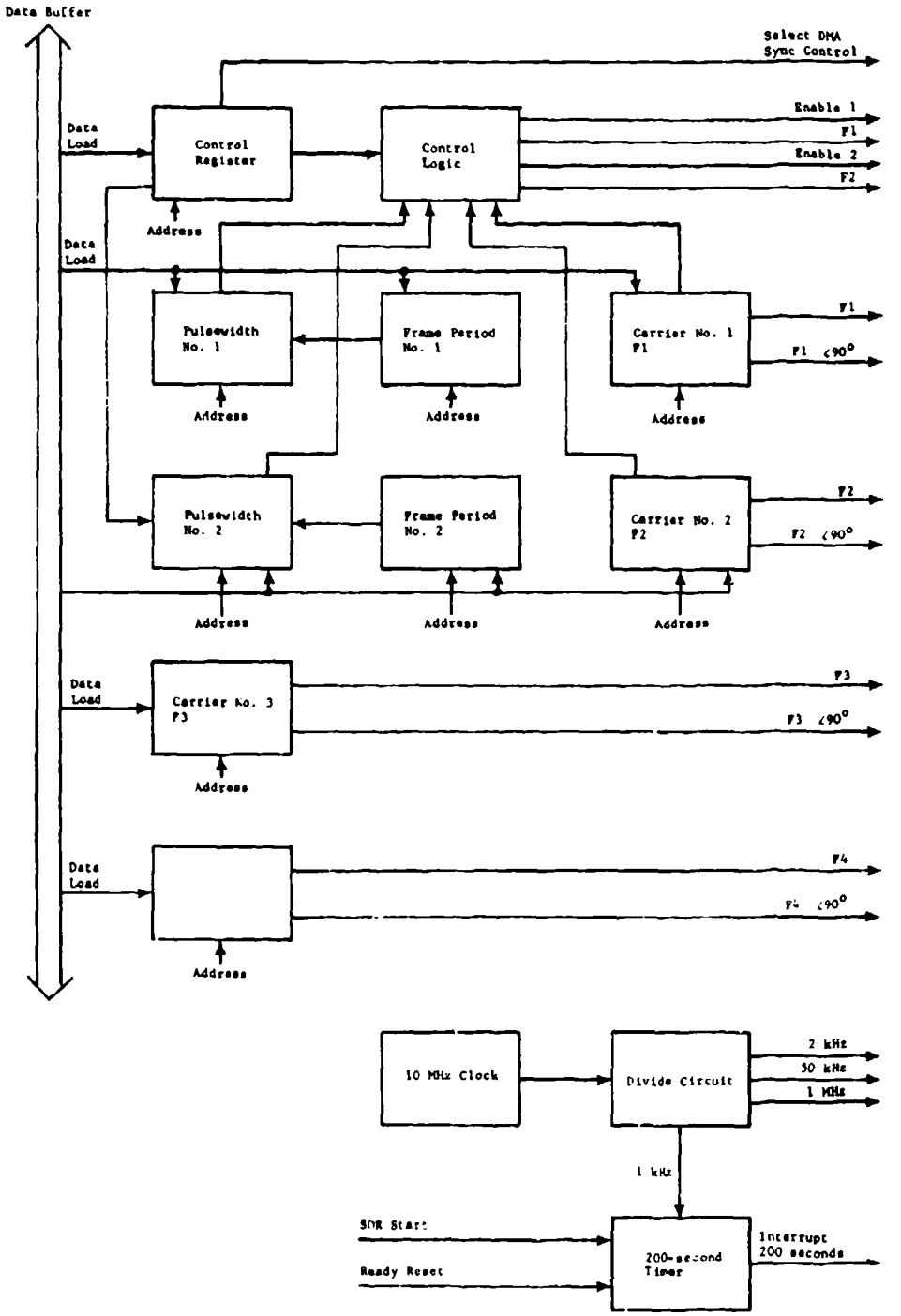


FIGURE 3-50. LOGIC FLOW, RADAR CONTROLLER, BOARD NO. 2

4. Data Control Register/Sync Data Control

The data control register is used to control the configuration of the data feeding to the A/D converter and the configuration of the frame period registers. The upper 8 bits are used to ON/OFF control the pulsed and cw generators, to control whether frame 2 has a fixed delay, and also to select whether frame 1 or frame 2 is used to initiate DMA transfer.

5. Synchronization Module Enable

The synchronization modules are enabled by the pulse width generators and provide the enable pulse to the envelope modulator module to form the transmitter pulses. The synchronization signal is also used to provide a square wave pulse to the analog tape recorder.

6. Clock

The clock provides the basic timing and reference signal generation required for the frame timing, carrier, and pulse width programmable counters. The basic clock is a 10 MHz crystal reference.

7. 200-Second Timer Function

The 200-second timer provides a system generated interrupt command to the computer 200 seconds after the start of run (SOR) if an externally generated end of run signal is not received. The timer is reset by the ready command and started by the SOR command.

3.2.7.3 Radar Controller Board 3 Functions

The logic flow of RCB 3 is shown in Figure 3-51.

1. Configuration Module Control

Interface with the configuration control module is via 8 lines of low-level active state transistor-transistor logic (TTL). The register is a 16-bit write register (which provides 8-bit expansion capability).

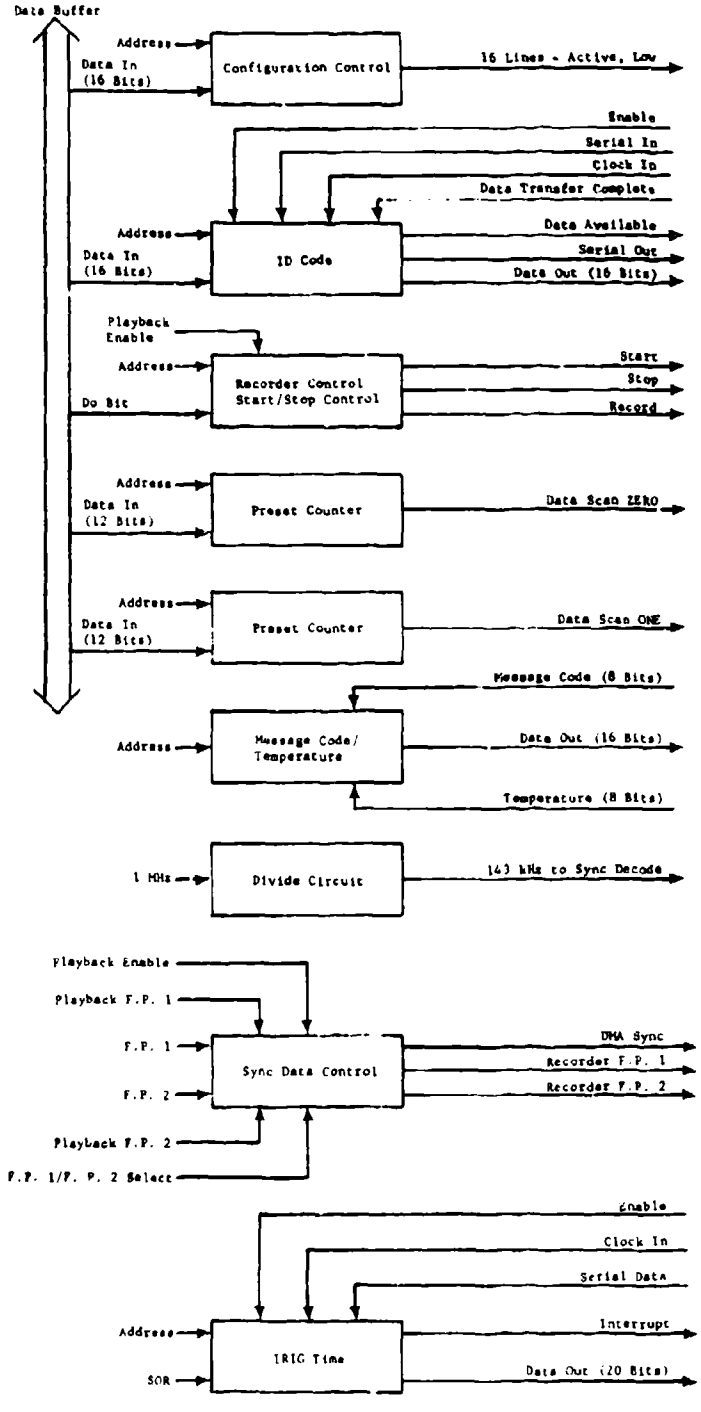


FIGURE 3-51. LOGIC FLOW, RADAR CONTROLLER, BOARD NO. 3

2. Message Code/Temperature Register Control

The message code/temperature register interface consists of 8 normally high lines. If any line goes low, the register will strobe the data and send an interrupt signal to the mini-computer. The upper 8 bits of the register are used for the message code; the temperature register occupies the lower 8 bits of the register. On command from the computer the temperature register accepts digital data from the temperature sensor A/D converter and strobes the data to the mini-computer.

3. IRIG Code Register Control

The IRIG code register is a constantly updated register which receives its input from the IRIG generator. Upon receipt of a start-of-run (SOR) command the IRIG code register completes any updating if in the middle of a cycle and then sends an interrupt command to the mini-computer. It takes two data words to transfer the 200 bits of the time code to the mini-computer. Updating remains halted until the two data words have been transferred to the computer. Upon completion of the transfer, register updating resumes.

4. ID Code Register Control

Timing of the ID code register is controlled by the sync decode module. During outgoing information cycles, a data available signal is sent. The sync decode module then controls the data transfer and sends a data transfer complete signal upon completion of the transfer. A controller busy signal is used during the active data transfer to prevent data from being entered into the register while data is being transferred out. The data-in cycle is controlled by a suitable interrupt command. Upon completion of a data transfer from the sync decode module, the ID code register sends an interrupt command. Upon completion of the data transfer to the mini-computer, the ID code register sends a READY-FOR-DATA signal to the sync control module to signal its readiness to receive data again.

5. Tape Stop/Start Control

The tape stop/start commands are provide by addressing the tape start/stop register. If a ONE is set into the D00 bit, the tape will start. It will stop in response to a ZERO in the D00 bit. The tape will also stop in response to an initiate signal to the controller.

3.2.8 Sync Decode Module

The sync decode module is packaged on two circuit boards. One board contains the analog and filter circuits for the analog tape recorder; the other provides circuits for the digital interface with the controller, digital decoding, and coding of the analog signals. Figure 3-52 is a block diagram of the sync decode module.

1. IRIG Time Generator Interface

The IRIG time generator interface is handled by a parallel-to-serial converter. The parallel register is loaded whenever the lowest-order bit(1-second increments) of the register changes state. A delay is then triggered to allow the data to stabilize; the parallel register contents are then transferred serially to the radar controller at a transfer rate of 144 kHz. The register can accept up to 20 parallel bits of information.

2. Word Information Network

When the data available signal is activated, the word code register first inhibits the SYNC-I signal; then sends out a 15-bit, 8 kHz start-of-word signal; and finally the 8 kHz bursts of pulses for ONES or ZEROES. These are sent at a rate of 250 Hz. Eight pulses are sent out for a ONE; four pulses are sent out for a ZERO. The register also clocks the primary controller and when the 16 bit word is complete it sends out a data transfer complete signal. (Figure 3-53 indicates the configuration used for data transfer). The data out signal is OR'd with the SYNC-I signal and sent to a conditioning operational amplifier used to enter the information on the magnetic tape.

3. IRIG-In

The IRIG is first filtered by a low-pass filter and then summed with the SYNC-II signal in a summing amplifier used to condition the signal for subsequent recording on magnetic tape. This configuration requires use of an IRIG format B signal with a 1 kHz carrier.

4. IRIG and SYNC-II DECODE

The signal from the magnetic tape is routed in parallel through low-and high pass filters. These are used to separate the IRIG and sync signals. The IRIG signal is then available for subsequent decoding (by an external decoder that is not included in the DAVSS design. The SYNC-II signal is then applied to an amplitude detector to provide the SYNC-II output command (SYNC-II decode pulse).

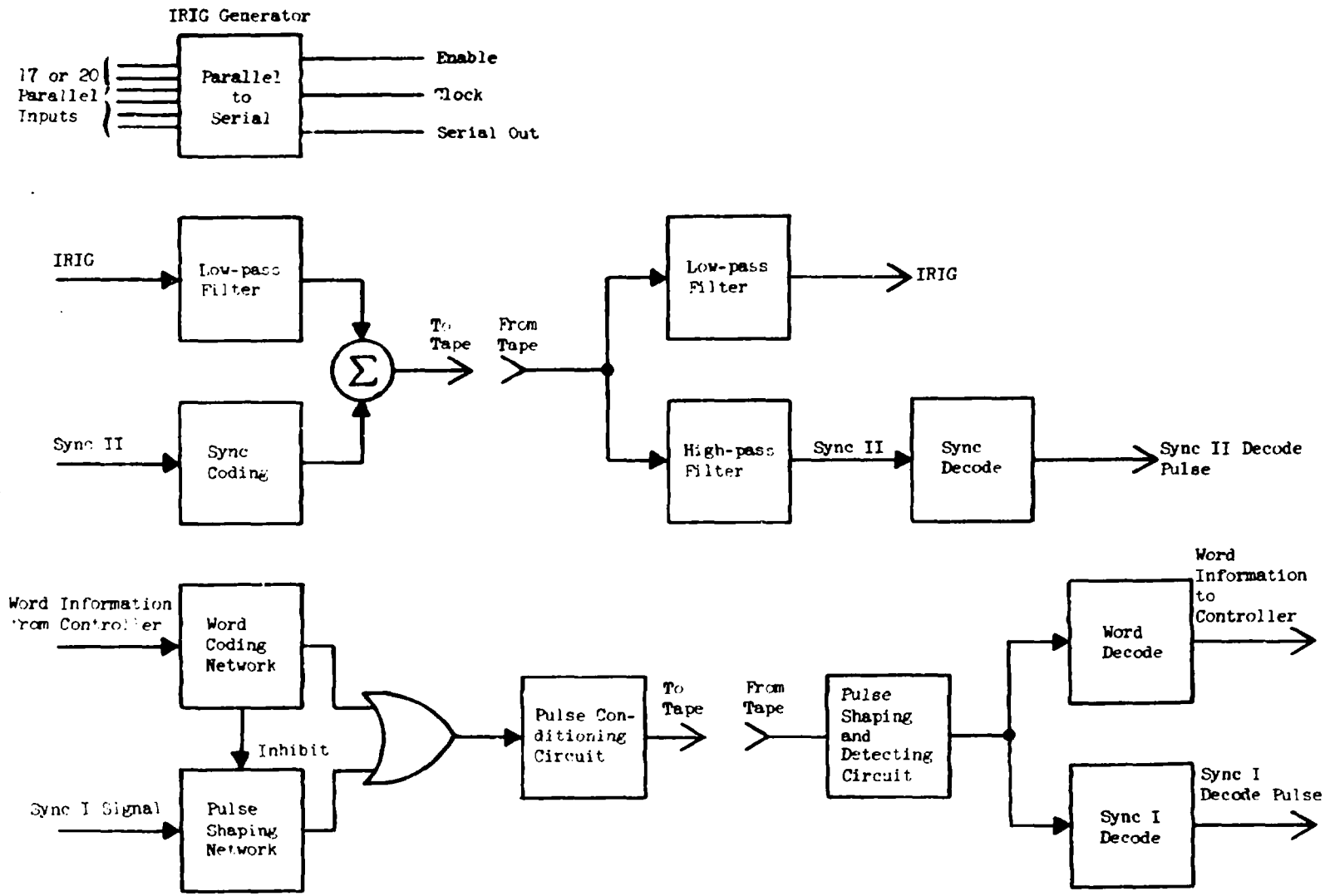


FIGURE 3-52. BLOCK DIAGRAM, SYNC DECODE MODULE

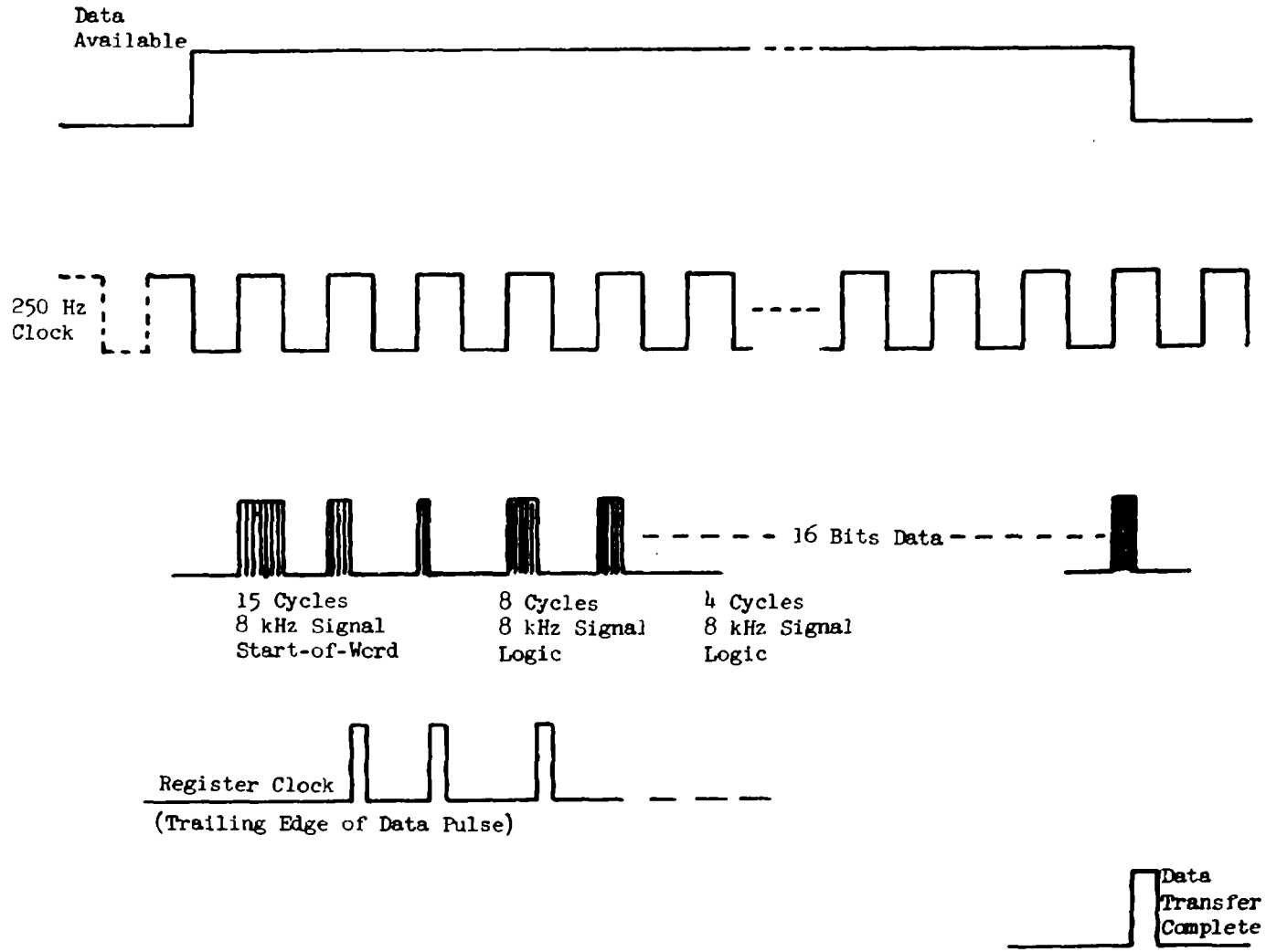


FIGURE 3-53. SYNC DECODE DATA TRANSFER CONFIGURATION

5. Word and SYNC-I Decode

The information from the tape recorder is passed through an amplitude detector to detect the 8 kHz pulses. A word decode module counts the number of bits in the word. If more than 12 are decoded, the register begins to send the data to the radar controller. All transfer timing is accomplished in response to the information acquired by decoding of the ONES and ZEROES. The SYNC-I decoder sends out a pulse at the start of every word whose information content is to be disregarded (those words that do not contain data, for example). Provision has been made for synchronizing word transfer with the frame sync signals should the need for this occur. The four words would be transferred in response to the first four frame sync signals.

3.3 DISPLAY SUBSYSTEM

The display subsystem consists of a CRT display unit and software provisions for a hard-copy display device. The displays are capable of presenting the following-listed information at the operator's option:

- Vortex Position — Horizontal versus vertical position as a function of time (CRT only).
- Vortex Position — Horizontal position as a function of time.
- Vortex Position — Vertical position as a function of time.
- Run Identification
- Pertinent Meterological Data
- Prompts to the Operator
- Intermediate Processed Data for Diagnostics.

3.3.1 CRT Display

The CRT display device is the DEC GT-40 graphics unit. This unit uses digital techniques and is, therefore, a stable system that requires only minimum adjustments. The display's vector function operates through a combination of digital and analog techniques, thereby providing a good compromise between speed and accuracy, and assuring precise digital vector calculation. The approach used to present and accumulate vectors is such that every point of the vector is available in digital form.

The end-point position is automatically and accurately held during plotting, thus preventing accumulated errors or drift. The vectors are of near constant velocity and are time-efficient regardless of length. Four different vector formats -- solid, long dash, short dash, and dot/dash -- are available in hardware. A smooth ramp deflection signal permits fast vectoring with moderate deflection bandwidth and power.

The GT-40 character generator has both upper and lower case capability with a complete repertoire of displayable characters. An automatically refreshed type display is used rather than a storage type so that a bright, continuous image with excellent contrast ratio is provided during motion or while changes are being made in the elements of the display. A blink feature is applicable (via hardware) to any characters or graphics drawn on the screen. A separate line clock in the display permits the GT-40 to be synchronized to a line frequency of 60 Hz. The CRT's resolution is precise enough to allow overprinting.

The GT-40 terminal includes logic for handling characters with descenders, such as "p" and "g". This enables such characters to be positioned correctly with respect to the text line. In addition to the 96 ASCII printing characters, 31 special characters are included. These are addressed through the shift-in/shift-out control codes. They include certain Greek letters, architectural symbols, and mathematical symbols. Characters can be presented in italics simply by selecting that feature through the status instruction bit. Eight intensity levels permit the brightness and contrast to be varied so that the display can be viewed under a variety of lighting conditions.

The GT-40 is integrated with the PDP-11/05 computer in a highly efficient way.

3.3.2 Hard-Copy Display

Software is provided in the system for operation of a hard-copy display device that has been provided as government-furnished equipment (GFE). The device is a Versatec Model 1100A electrostatic printer/plotter, designed for plug-in compatibility with any PDP-11 minicomputer. The Model 1100A unit is basically a high-speed line printer/plotter that uses an electrostatic printing technique. The writing head, in which 1024 individually addressable writing electrodes are incorporated, is fixed in position. As paper passes over the writing head any or all of the writing electrodes may be activated to deposit a charge on the coated paper. The charged paper then passes over a liquid toner that contains carbon particles. The particles are attracted to the charged areas of the paper, causing the appearance of black dots. A heating element fuses the carbon particles to the paper and assures delivery of a dry copy of the printout.

The entire ASCII character set (including both the upper and lower case alphabets) can be printed in 132 columns per line at a rate of 500 lines per minute.

Detailed specifications of the hard-copy display device are listed in Table 3-8.

TABLE 3-8

VERSATEC PRINTER/PLOTTER SPECIFICATIONS

Plotting	
Plotting Area	10.24 inches square
Total Writing Points	1024
Writing Point Spacing	100 per inch
Vertical Line Spacing	100 per inch
Input	8-bit parallel bytes
Data Transfer Rate	500K bytes per second
Plotting Speed	122,880 dots per second
Memory	One-line buffer (1024 bits)
Printing	
Columns	132
Character Spacing	12.5 per inch
Character Font	7 by 9 dot matrix
Character Generator	Read-only memory (ROM)
Print Rate	500 lines per minute
Input Code	7-bit ASCII (USAS x 3.4-1968), parallel, no parity
Character Set	96
Memory	One-line buffer (132 characters)
Dimensions	
Width	19 inches
Height	38 inches
Depth	18 inches
Weight	160 pounds
Paper Drive	Incremental
Paper Advance Speed	1.20 inches per second
Writing Spot Size	0.0075-inch diameter
Power Input	
Volts	115
Watts	600
Phase	Single

3.4 DATA STORAGE SUBSYSTEM

This subsystem consists of two magnetic tape recorder/reproducers. A 28-track direct recording analog magnetic tape recorder is used to record twenty-four (24) channels of received signals, two time-reference and 1D channels, and one channel for voice commentary regarding run identity, array configuration, etc. One channel is unused.

A 9-track digital magnetic tape recorder in the data storage subsystem is used to record the identity of the run, the array configuration, the time delays as calculated by the minicomputer, the vortex tracks as calculated every two seconds, and the meteorological data (sign, plus three decimal digits from each of 10 sensors) when fed into the system.

Each unit is described in the following paragraphs.

3.4.1 Analog Tape Recorder

The analog tape recorder in the data storage subsystem is the Bell and Howell CPR 4010/3700B portable magnetic tape recorder/reproducer. This unit is a rugged, portable, instrumentation-quality recorder/reproducer capable of providing laboratory-caliber performance in a field application. It is fully Inter-Range Instrumentation Group (IRIG) compatible. It is rack mounted and contains 28 channels of direct record and play back electronics. It has seven speeds, ranging from 15/16 to 60 inches per second. Control of the unit is either manual (at the unit) or remote (from the data acquisition subsystem).

The analog tape recorder accepts inputs from the signal processor configuration control module as follows:

- 24 unfiltered signals received by the Doppler acoustic radar subsystem
- Frame sync signals
- Start/Stop commands (relay closures)
- Start and End of Run (SOR and EOR) event signals
- Start of run time
- Run numbers
- Mode indicators

- Carrier frequency and modulation information pulse length and pulse repetition frequency
- Voice commentary from the audio system.

The analog tape recorder provides outputs to the signal processor configuration control module as follows:

- 24 array signal channels
- Frame sync
- Start of run
- Mode configuration
- Run number
- Carrier frequencies

and provides voice commentary playback to the audio system.

At a tape speed of 1.875 inches per second (ips) and with each run taking 200 seconds, approximately 50 to 80 runs can be recorded per reel of tape.

Pertinent specifications of the analog recorder are summarized in Table 3-9.

3.4.2 Digital Tape Recorder

The digital tape recorder in the data storage subsystem is the Digital Equipment Corporation (DEC) TU-10/EA (9 track) transport. This unit interfaces with the DEC PDP-11 minicomputer via a DEC TM-11 control unit. The TU-10 transport is a high-performance, low-cost, industry-compatible magnetic tape transport. Transfer of information between the PDP-11 and other computers is possible because the TU-10 reads and writes in an industry-compatible format.

TABLE 3-9

ANALOG RECORDER SPECIFICATIONS

Number of Tracks	28
Head Configuration	Per IRIG 106-71
Tape Speed	15/16 to 60 inches per second
Tape Speed Accuracy	± 0.15% all speeds
Control	Manual and remote
Tape Width	1 inch
Start Time	4 seconds, maximum, at 60 inches per second
Stop Time	3 seconds, maximum, at 60 inches per second
Fast Forward/Reverse	600 feet per minute
Fail Safe	Automatic shut off for power failure, tape breakage, or end of tape (EOT)
Flutter	Per IRIG 106-71
Heads	Per IRIG 106-71
Harmonic Distortion	1% 3rd harmonic distortion at 30 inches per second and normal record level
Input Level	0.5 to 20 volts, peak-to-peak
Input Impedance	75 ohms shunted by 50 picofarads (20K minimum with terminating resistor removed)

TABLE 3-9 (CONCL'D)

ANALOG RECORDER SPECIFICATIONS

Output Level	4 volts, peak-to-peak, into 600 ohms single-ended
Output Impedance	Less than 75 ohms
Equalization	Internal, automatically selected by speed
Reel	10 inch
Mounting	Relay rack.

The digital tape recorder records the identity of the run in response either to keyboard inputs or signals from the central processor. It records the mode configuration, the start of run time, the A/D converted outputs of the filter banks, the computed doppler discriminants, the vortex tracks as calculated every two seconds, and the meteorological data.

The digital tape recorder is also used to load the system operating program into the minicomputer.

Pertinent specifications of the digital recorder are summarized in Table 3-10.

TABLE 3-10

DIGITAL RECORDER SPECIFICATIONS

Tape	0-5 inch wide, industry standard
Tape Read/Write Speed	45 inches per second
Rewind Speed	150 inches per second (approximately 3 minutes for 2400-foot reel)
Packing Density, 9-channel	800 bits per inch
Maximum Transfer Rate	36,000 characters per second
Inter-record Gap	0.75 inch or greater
Recording Mode	NRZ
Magnetic Head	Dual gap, read after write
Data Transfer Method	Non-processor request (Direct Memory Address, DMA--cycle Stealing)
Beginning of Tape/End of Tape (BOT/EOT) Detection	Photoelectric sensing of reflective strip
Skew Control	De-skewing electronics eliminate static skew
Write Protection	Write protect ring sensing
Data checking Features	Read after write parity checking of characters. Longitudinal redundancy checks (7-and 9-channel)
Programmable Commands Accepted by Transport	Rewind and Go Off-line Read Write Write End-of File Character Space Forward Space Reverse Write with Extended Inter-record Gap Rewind to BOT.

TABLE 3-10 (CONCL'D)

DIGITAL RECORDER SPECIFICATIONS

Extended Features	Self-test of control with recorder off-line
Local Transport Controls	On-line/Off-line Forward/Reverse/Rewind Unit Select Power On/Off Start/Stop Brake Release/Load
Design Features	Industry standard compatibility Power failure interlocks to prevent tape damage or data loss High capacity (10-1/2 inch diameter reels can hold up to 2400 feet of tape)
Mechanical	Relay rack mounting
Compatibility	TSC PDP-10 computer format.

3.5 SOFTWARE

3.5.1 General

The software system is required to perform three functions: DAVSS operation, DAVSS control, and data processing. The system consists of an operating system and two application programs, one for each configuration (cw or pulsed). All programs are initially loaded into the PDP-11 from a 9-track tape, using a bootstrap loader.

The operating system permits the operator to initialize the system by prompting him for various parameter values. A GT-40 display screen and associated keyboard are used for all operator-system communication. Other portions of the operating system allow the operator to start and stop a run and supply the radar subsystem controller with the parameters needed for signal processing. Other functions of the operating system include:

- Power Fail and Restart Handling
- Interrupt Processing
- I/O processing
- Conversion
- Selection of Application Program.

The interrupt processing includes the handling of interrupts from:

- The operator (keyboard)
- The radar subsystem controller
- The hard-copy printer
- The 9-track tape unit
- The clock.

I/O processing includes formatting and control routines for:

- The keyboard
- The GT-40 display

- The hard-copy printer
- The 9-track tape unit.

Conversion routines include:

- ASCII to binary
- Binary to BCD.

Based on the operator's choice, the operating system selects the particular application program desired (cw or pulsed), and then turns over control to that program along with any parameters required. Upon completion of processing, the system checks for operator's requests, honors valid requests, and repeats the cycle until the operator stops the run, or 200 seconds have elapsed.

3.5.1.1 CW Configuration

The application program for the cw configuration performs the following functions:

- Receives initialization parameters from the operating system
- Initializes the digital tape
- Upon receipt of an operator command, commences vortex tracking
- If requested, dumps continuous raw digital data, discriminant data, or vortex track data on digital tape
- Continuously displays vortex locations, discriminant or raw data
- If requested, prints vortex locations, or a frame of discriminant or raw data

Vortex tracking itself is, of course, the primary function of the cw software. Given 144 spectral data points, the software validates the return and, if valid, determines the vortex locations. These locations are saved for printing and/or display.

3.5.1.2 Pulsed Configuration

The differences between the pulsed and the cw programs are in the vortex tracking and the output formatting. Given 72 spectral data points for each delay value, the software for the pulsed configuration validates the returns, and if valid, determines the vortex locations. These locations are saved for printing and/or display.

3.5.2 Operating System

The following set of descriptions and flow diagrams present a general outline of the DAVSS software. It is intended to be an overview of the software system operation. In some cases, a fair amount of detail is presented in the flow diagrams when it is felt that this could aid in the operator's understanding of his control of the system. Other large sections of code are described only by the function which they perform without reference to method. Still other lower level "service" routines are not described at all. Examples of this are the floating point and trig function routines.

The complete software system is defined by the program listing which is too voluminous to be part of the final report. These routines and programs are all written in AVMOTS* assembly language which is quite similar to DEC PAL II language. Within a program, any symbolic references to locations defined in another program and contained by that program are resolved by the AVMOTS linkage editor. This represents a very powerful tool and it has been used extensively.

The flow charts of Figures 3-54 through 3-58 are intended to be self-explanatory, however, a short description will aid in understanding the connections between various routines.

The main program (MAIN) is flowcharted in Figure 3-54. This chart shows very little program detail. Large portions of code are indicated only by their function. Examples are: Perform Requested Hardware and/or Software Change, Search for Vortex Return(s), and Form Position Solution.

The chief flow routing parameter in MAIN is called the system state. Its value is determined by either the status of the software or external events. The events may be operator actions or signals sent to the DAVSS controller. The normal transition route of the system is as follows:

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* AVCO Modular Test Station.

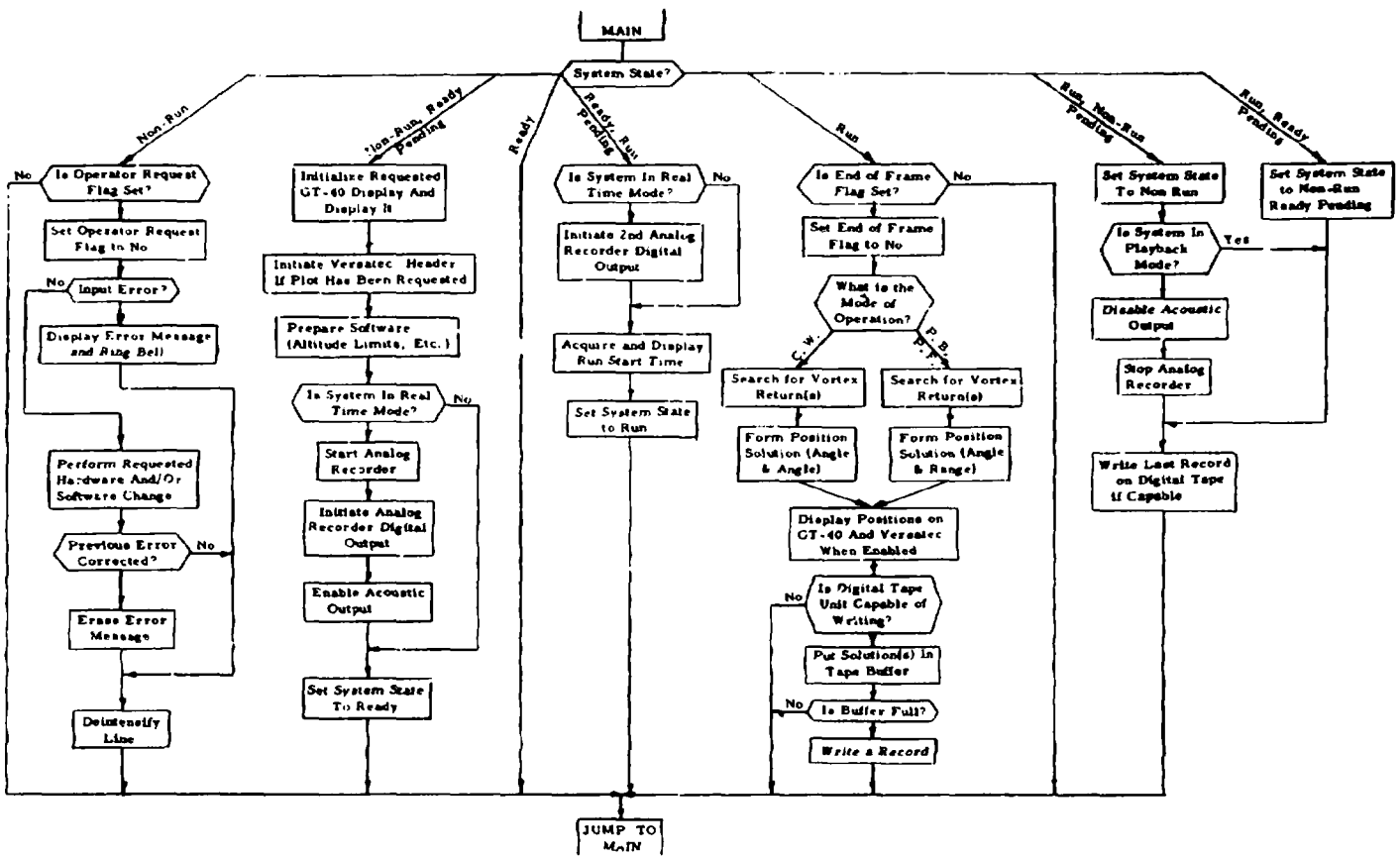


FIGURE 3-54. FLOW CHART, MAIN PROGRAM

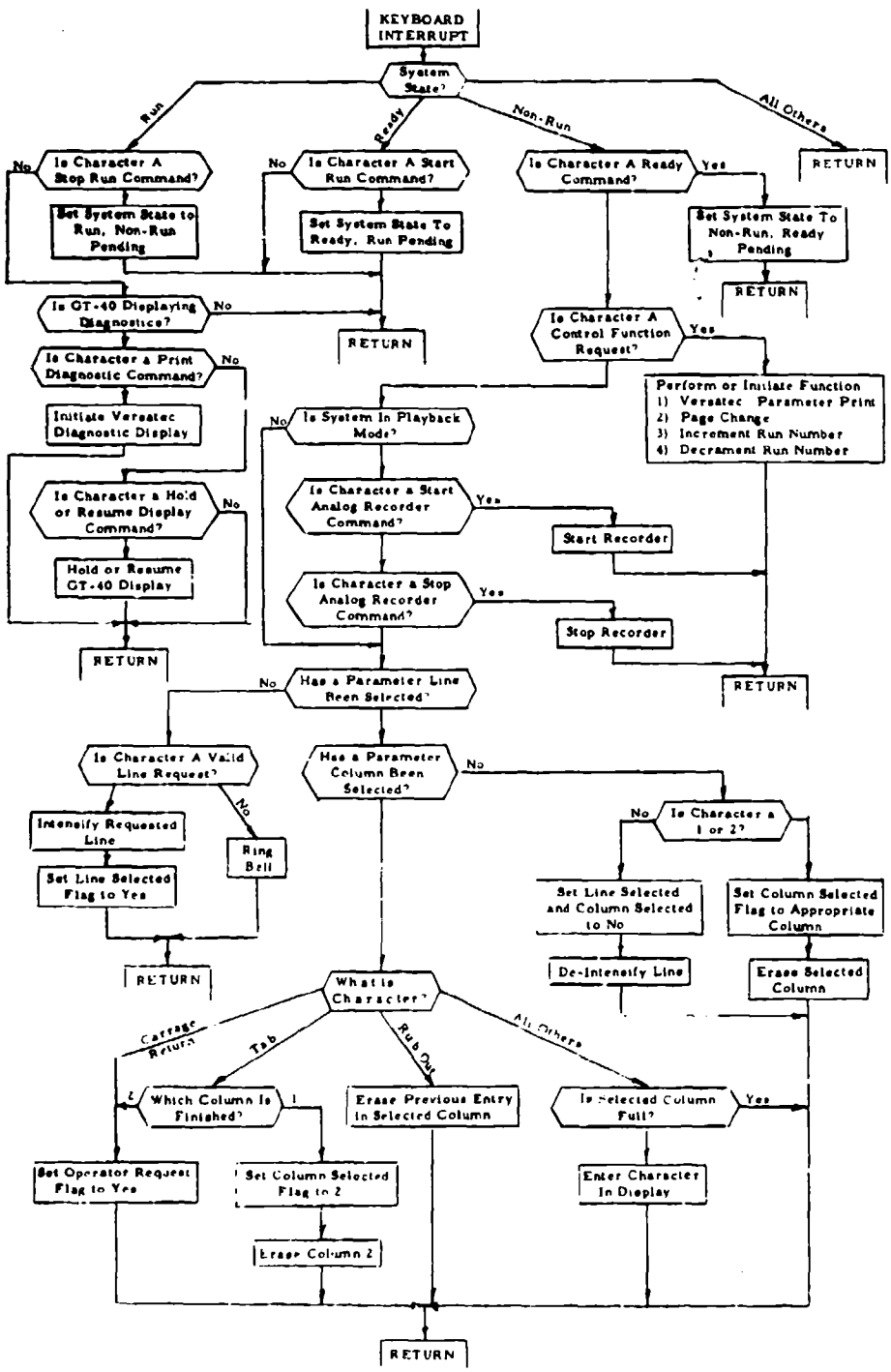


FIGURE 3-55. FLOW CHART, KEYBOARD INTERRUPT

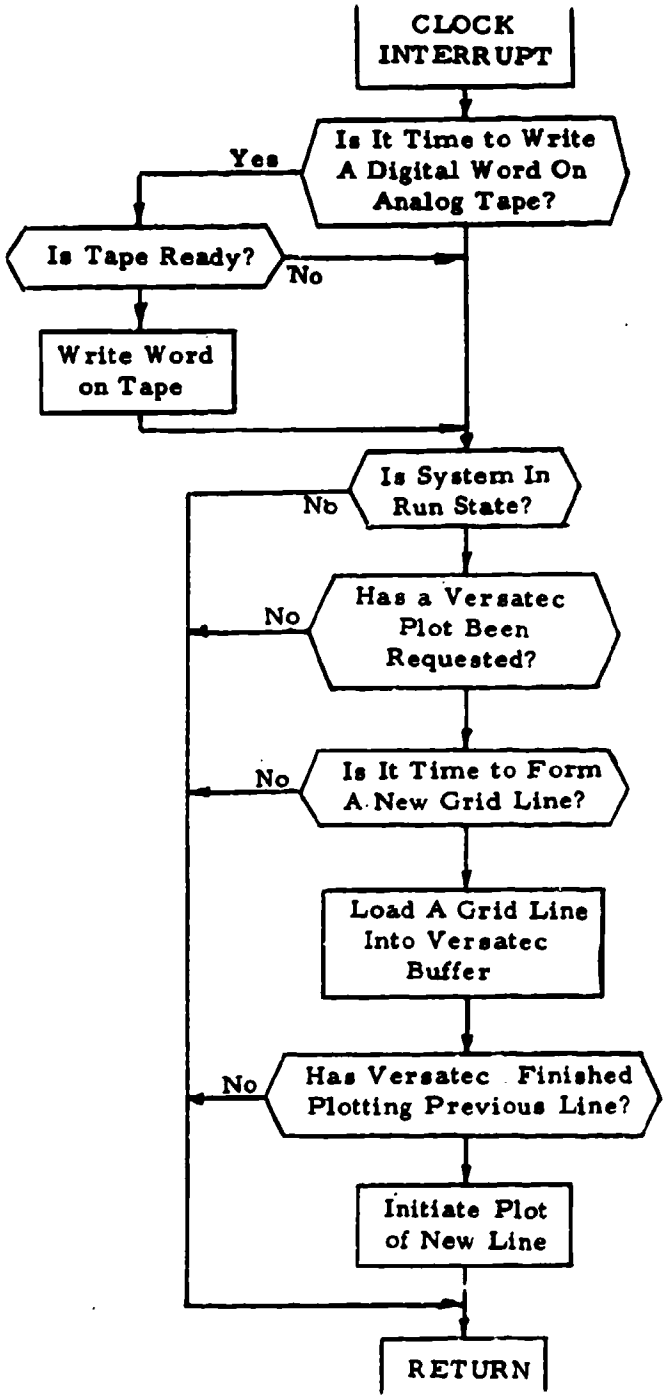


FIGURE 3-56. FLOW CHART, CLOCK INTERRUPT

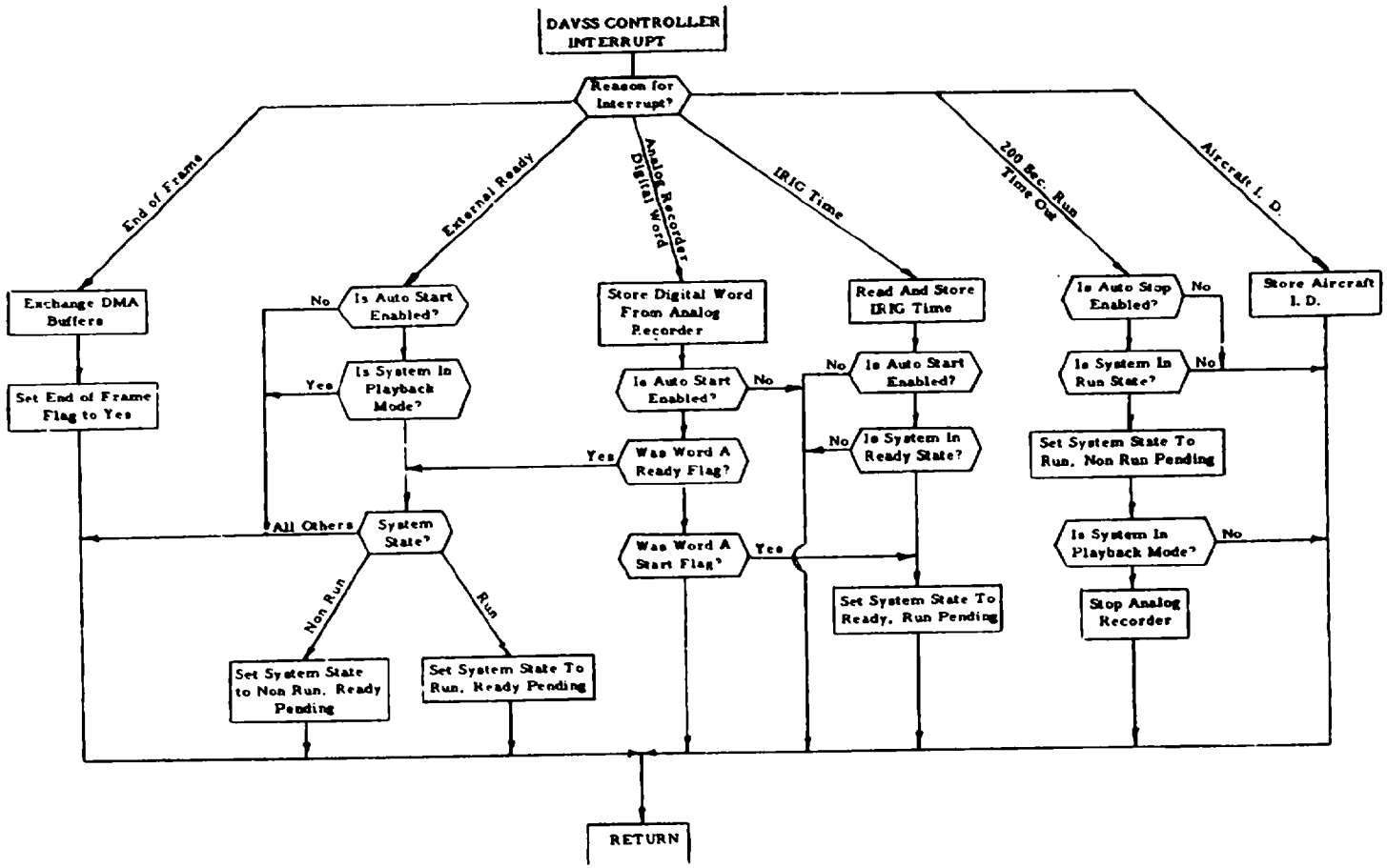


FIGURE 3-57. FLOW CHART, DAVSS CONTROLLER INTERRUPT

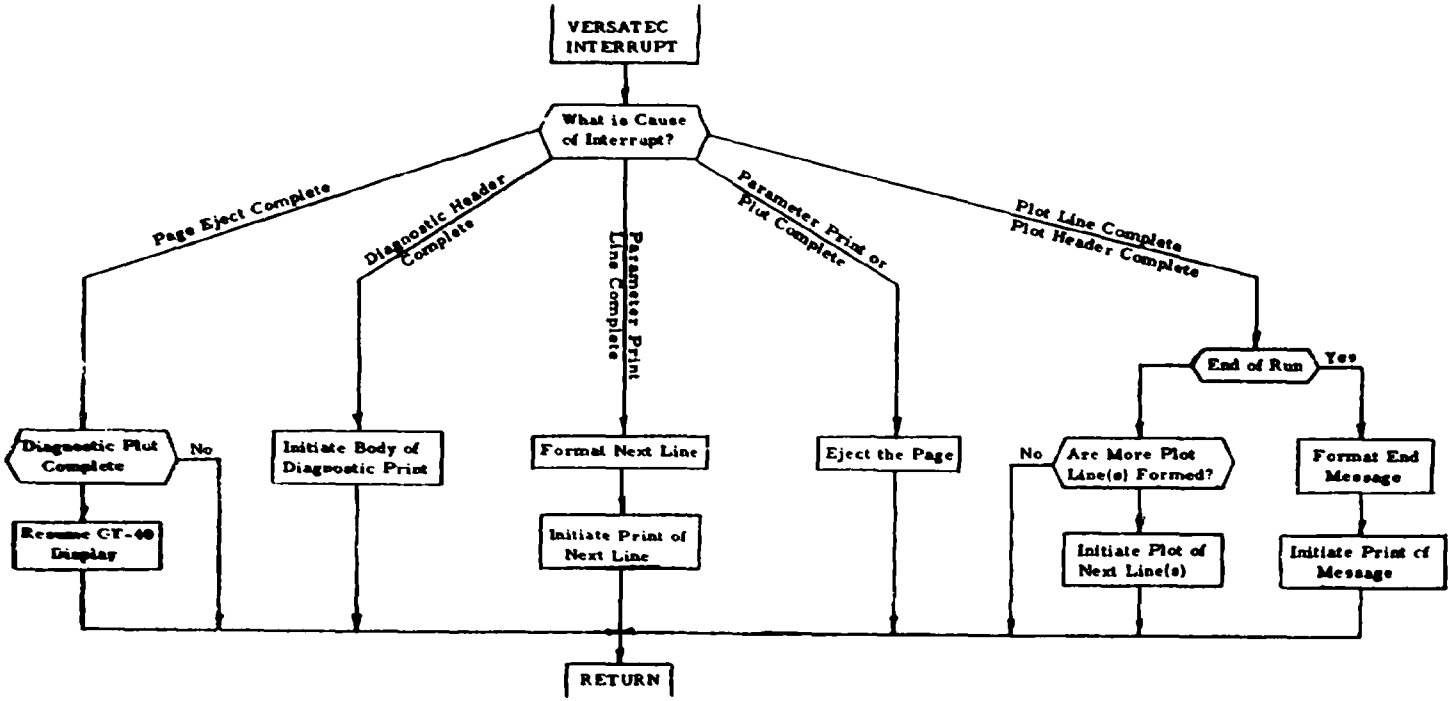
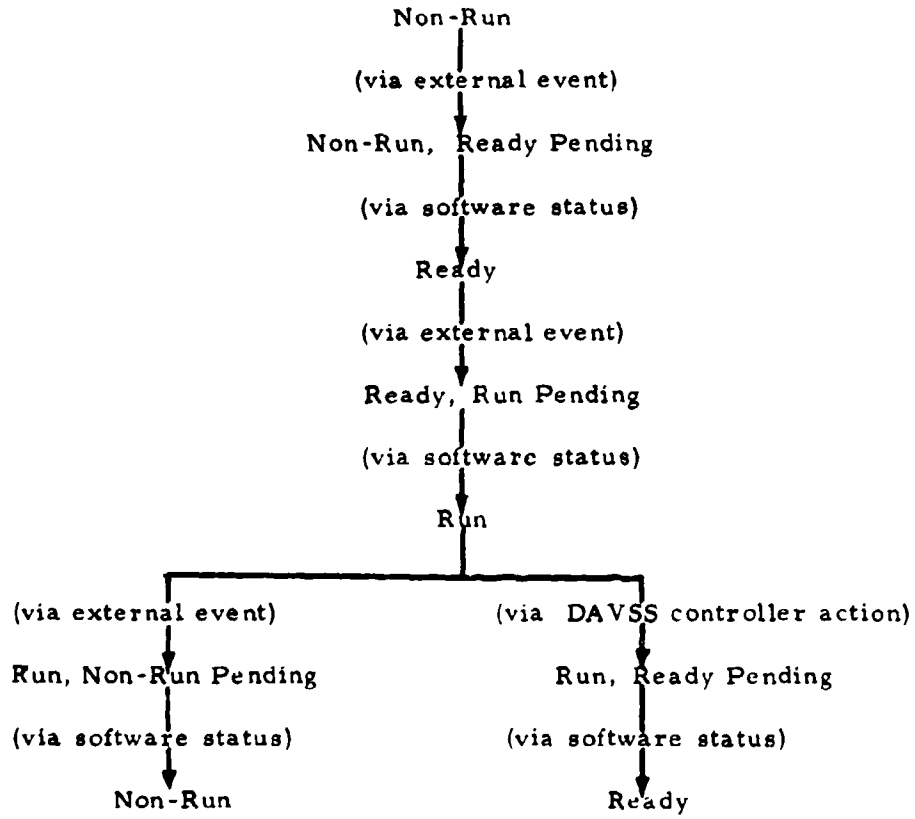


FIGURE 3-58. FLOW CHART, VERSATEC INTERRUPT



The only exit from the loops of MAIN is by a hardware/software action called an interrupt. When an interrupt is issued, the program status is stored and control is transferred to the appropriate interrupt routine. When the interrupt routine has finished, the old program status is restored and control passes back to the interrupted routine. Using this method, various parameters in the MAIN program (such as system state) may be changed. Four devices are capable of issuing interrupts. They are the keyboard, the DAVSS controller, the clock, and the Versatec print/plotter.

When the operator presses a key on the keyboard, an interrupt is issued and program control passes temporarily to the routine charted in Figure 3-55. This routine is treated in considerable detail in the flow chart since reference to it enables the operator to determine what effect certain of his actions will have on the system.

The three other interrupt routines: Clock, DAVSS controller, and Versatec are charted in Figures 3-56 through 3-58.

4. SYSTEM OPERATION

The purpose of this section is to describe the DAVSS system operation. Paragraph 4.1 describes the principal operating modes and the data organization, processing, and search routines which detect and locate vortices in the system field of view. Paragraph 4.2 describes the display formats which are available for use by the operator on both the CRT and hard copy display subsystems. Paragraph 4.3 describes the basic operating procedure to load the system operating program, initialize parameters, and collect vortex detection and tracking data. Specific step by step instructions are contained in the Operating Manual and are not included as part of this report.

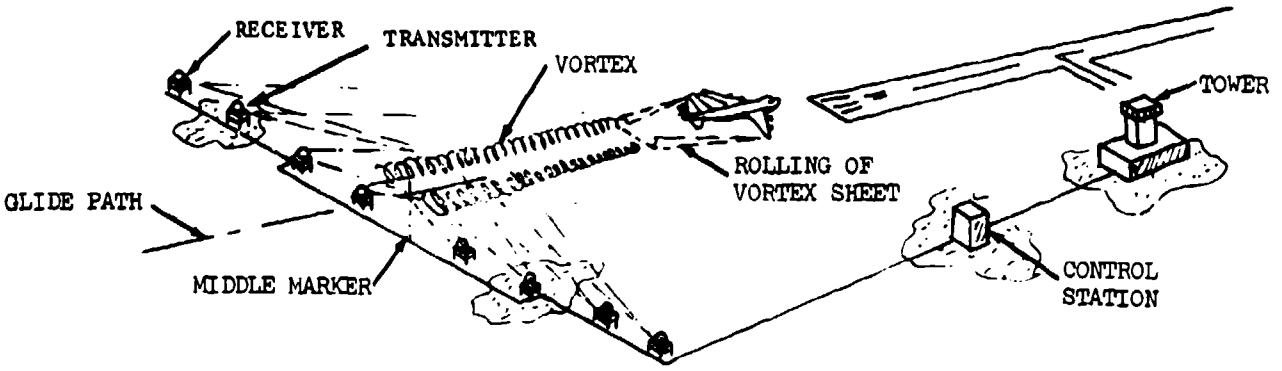
4.1 PRINCIPAL OPERATING MODES

The Doppler acoustic vortex sensing system is capable of operating in any of two alternative modes--cw and pulsed, and in any of three alternative siting configurations--bistatic forward scatter, bistatic backscatter, and monostatic backscatter.

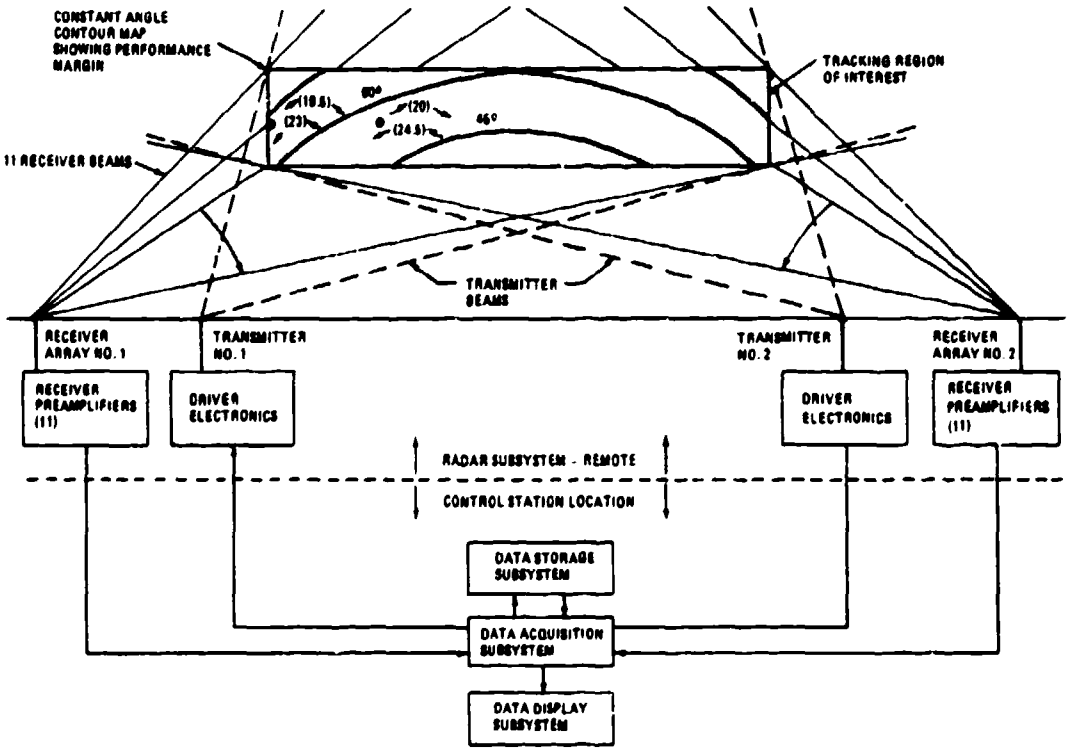
4.1.1 CW Forward Scatter Bistatic Operation

When the system is to be operated in the cw mode and in a bistatic forward scatter configuration, a transmitting and a receiving antenna assembly are set up on each side of the runway centerline extension (relative to the glide path cross sectional zone of interest at that location) as shown in Figure 4-1. Each transmitter elevation angle, elevation beamwidth (37°, 45°, or 60°), and location are selected so that the entire zone of interest can be uniformly illuminated (within 3 db of boresite angle gain). Thus T_1, illuminates the whole zone of interest; and vortex scattered energy is detected in several of the 12 beams of receiver R_2 on the other side of the runway centerline extension. Conversely, transmitter T_2 also illuminates the region; and vortex scattered energy is received and detected at receiver R_1. Independent estimates of the elevation angles of the left and the right circulating vortex are made in receiver 1 and in receiver 2. These may be designated Φ_{1L}, Φ_{1R}, Φ_{2L}, and Φ_{2R}. The intersection of Φ_{1L} and Φ_{2L} determines the location of the left circulating vortex while the intersection of Φ_{1R} and Φ_{2R} locates the right circulating vortex.

Since the vortex can have considerable extent, and since its scattering cross section per unit area may not be constant across that extent, Doppler discrimination is used to determine the location of the vortex



(a) Artist's Concept



(b) Block Diagram

FIGURE 4-1. DAVSS CONFIGURATION

center. In addition, since two vortices (one with left circulation and one with right circulation) will often be simultaneously present within the field of view, Doppler discrimation must also be utilized to correctly match the angular location of the left circulation vortex in R_1 with the left circulation vortex in R_2 and the right circulation vortex in R_1 with the right circulation vortex in R_2.

Doppler discrimation is accomplished by comb filtering the outputs of the twelve beams in each of the two receiver assemblies. From a combination of theoretical modeling studies, analysis of published Doppler acoustic data, and examination of our own experimental backscatter data, it was determined that six comb filters per receiver beam channel are sufficient to provide the Doppler discriminants necessary: (1) to distinguish right from left circulation, and (2) for angular location of the vortex center. A combination of three algorithms: spread, intensity, and skew are used to transform the comb filter output amplitudes into Doppler discriminants. Figure 4-2 and 4-3 show the functional relationship between each of two of the discriminants – skew and intensity – and the angular displacement of a receiver beam from the center of a right circulation vortex. The left circulation vortex presents a similar picture but the skew discriminant has the opposite slope.

Figure 4-4 presents a data processing flow diagram for the cw mode. It reflects the requirement that, at any given time, the data from 24 microphone outputs must be processed to determine the detected signal strength and the Doppler characteristics (spread, intensity, skew). To accomplish this, each microphone output is high-pass filtered, preamplified, low-pass filtered, and further amplified before it is transmitted from the remote radar subsystem to the data acquisition subsystem. At the DAS, each microphone signal channel is filtered, translated, and notch filtered to reduce the direct ground wave signal feed through, and retranslated to a frequency band where the computer controlled six comb filters are positioned. The outputs of the six filters for each of the 24 channels are processed in hardware to detect and integrate the resulting signals.

The six filters of each succesive receiver beam are simultaneously sampled and the data is input to the intensity, spread, and skew hardware algorithm circuit. The three resulting discriminant values are sampled and A/D converted prior to the mini-computer. Capability also exists to bypass the hardware algorithms and transfer raw filter

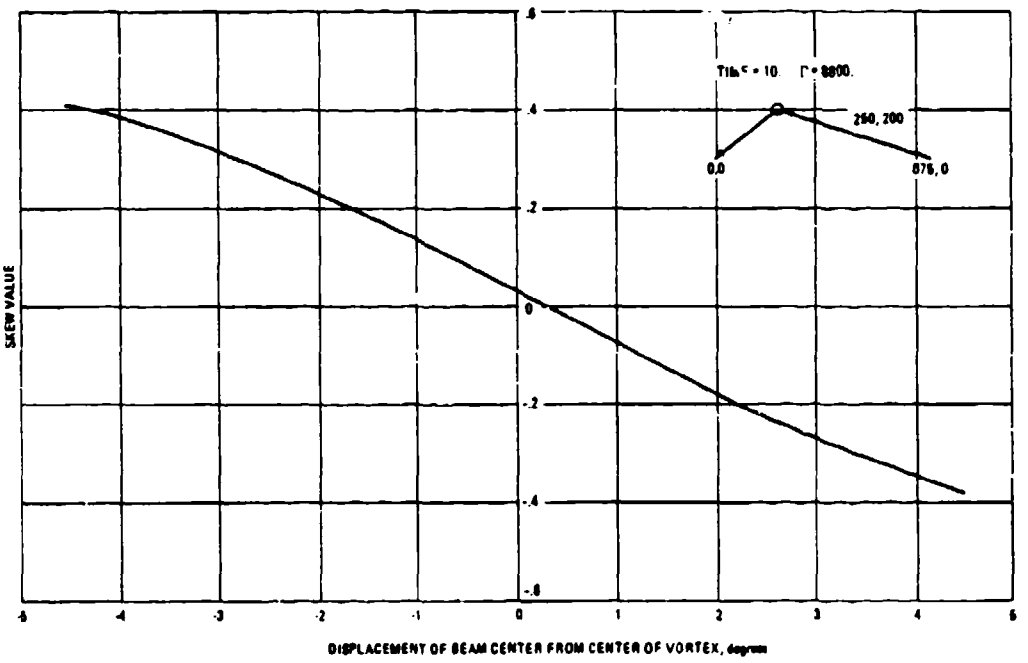


FIGURE 4-2. SKEW VERSUS LOOK ANGLE

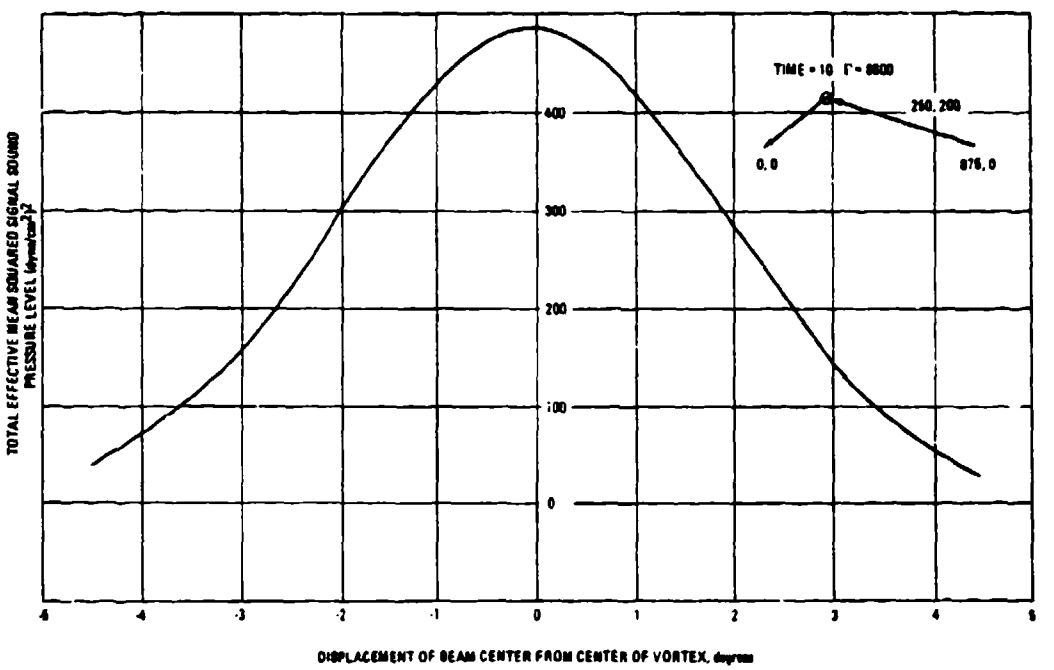


FIGURE 4-3. INTENSITY VERSUS LOOK ANGLE

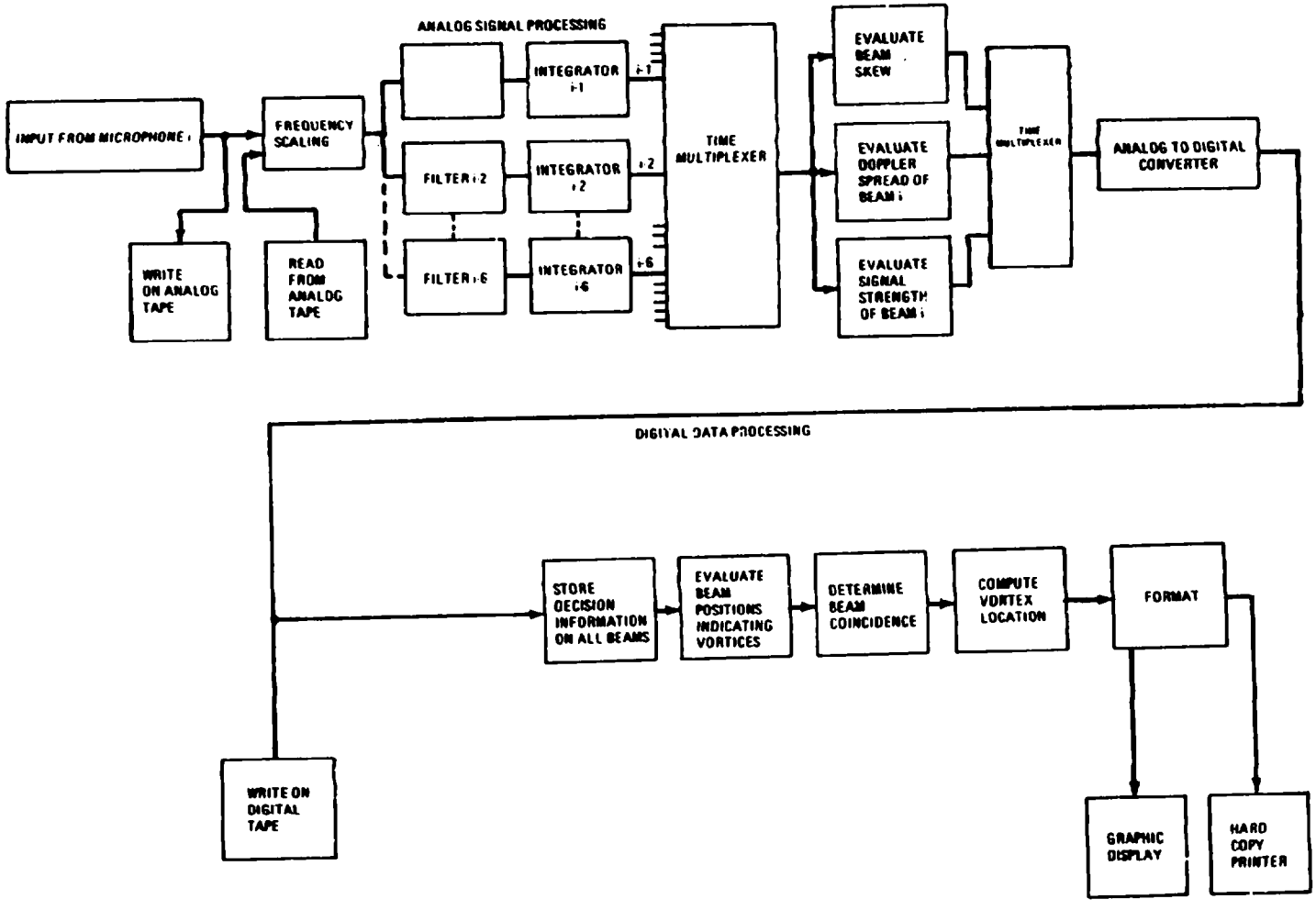


FIGURE 4-4. DATA PROCESSING CW MODE

data to the mini-computer. The data sequences for these two options are shown in Figure 4-5.

Hardware is provided for all 24 channels so that a total of 144 filtered samples result for each sample period in the cw mode. The comb filters have bandwidths variable under computer control from about 160 Hz to 30 Hz so that their outputs could be independently sampled every 8 ms to 33 ms, respectively. However, since no range capability exists for the cw mode, and since the vortex will probably remain relatively stationary for periods up to 0.2 seconds (depending on the ambient wind), post detection integration is realized by increasing the detector time constant on each filter channel. The intersample period is also increased to near the 0.2 second period to reduce redundant data. By this method post detection integration gains of nearly 14 db for the 160 Hz filters and 9 db for the 30 Hz filters accrue.

The sampling rates are determined for the data rate required. When slower data rates are utilized such as in the cw case, the period between successive scans of the 144 channels is increased by lengthening the time between the scan-enable pulses. The sampling rate within each scan remains the same as does the A/D conversion rate.

Figure 4-5 shows the data sequence of both the raw filter data and the discriminant data, either of which is transferred to the mini-computer by direct memory address (DMA). The raw filter data option is only used for diagnostic display purposes and is described in paragraphs 4.2.1. The discriminant data option can also be used for diagnostic display and is the data source for vortex detection and tracking. For detection and tracking, each receiver is treated separately so that the first 36 words represent data for receiver 1 and the second 36 words represent data for receiver 2. A simple search routine is utilized to determine vortex presence and location. The sum of intensity and skew for each of the 12 beam positions is formed. The two highest values among the twelve numbers are chosen, and the form of the skew profile about these is utilized to determine the left and the right circulating vortex. Having identified the two vortices each with its respective elevation angle for one receiver, the same procedure is followed for the second receiver. The four data points are then combined to form the two vortex locations by the following relations:

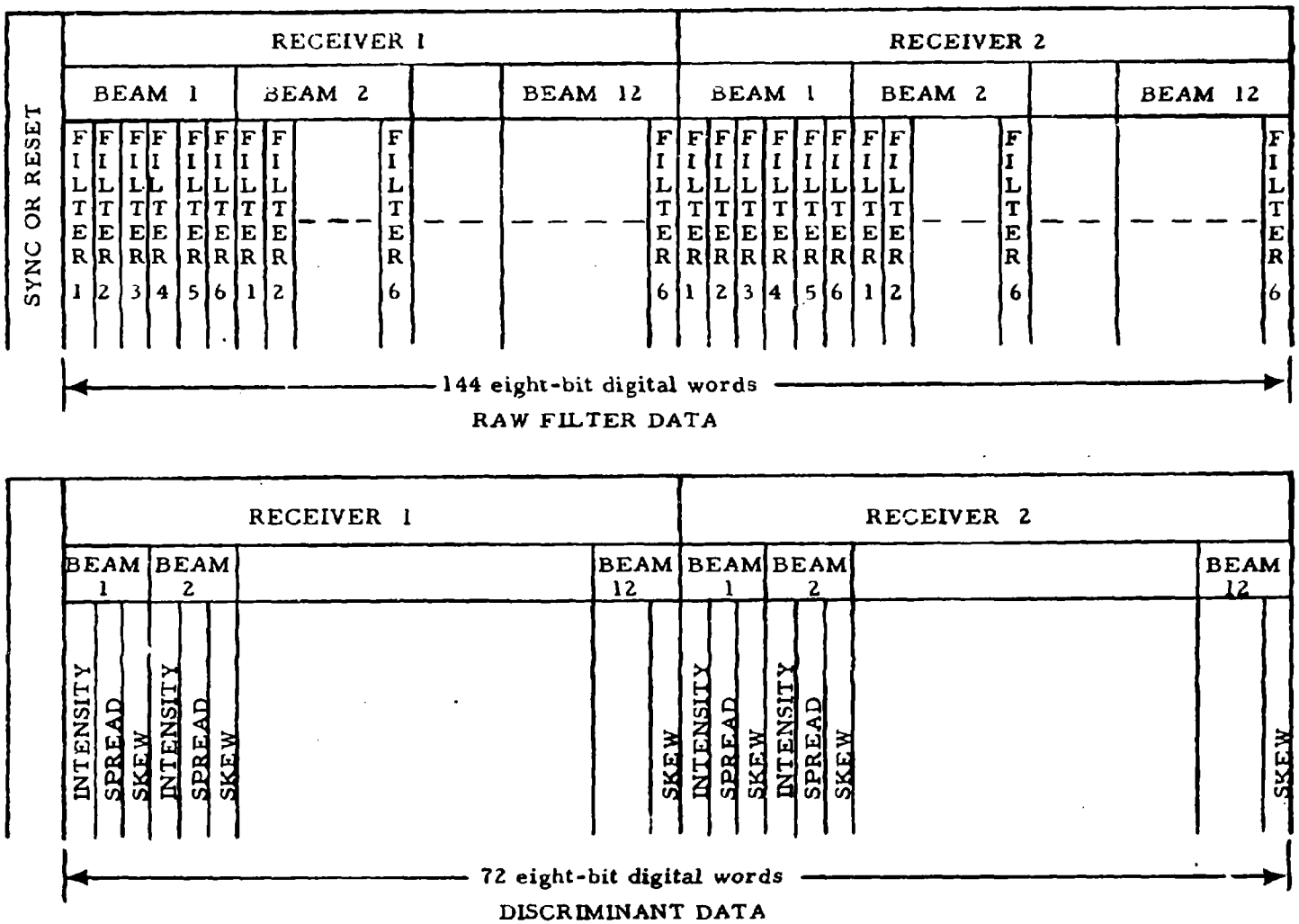


FIGURE 4-5. DATA SEQUENCES

$$x_R = \frac{b}{2}\left[\frac{\sin(\phi_{1R} - \phi_{2R})}{\sin(\phi_{1R} + \phi_{2R})}\right]; \qquad x_L = \frac{b}{2}\left[\frac{\sin(\phi_{1L} - \phi_{2L})}{\sin(\phi_{1L} + \phi_{2L})}\right]$$

$$y_R = b\left[\frac{\sin\phi_{1R}\sin\phi_{2R}}{\sin(\phi_{1R} + \phi_{2R})}\right]; \qquad y_L = b\left[\frac{\sin\phi_{1L}\sin\phi_{2L}}{\sin(\phi_{1L} + \phi_{2L})}\right]$$

where b is the distance between the receivers which are equally displaced from the runway centerline and ϕ_{1R}, ϕ_{1L}, ϕ_{2R}, ϕ_{2L} are the four elevation angle determinations of the left and right vortex in receiver 1 and 2 respectively.

The problems with noise and false alarms are treated by making use of the sample-to-sample history and the aggregate signal level in all the beams. The fact that the system is being dominated by aircraft noise immediately before and after aircraft passage is detected in the software by summing all the intensity and spread values. If the sum exceeds an empirically determined value, the system is considered dominated by aircraft noise and no attempt at detection is made. To reduce the false alarm rate for low signal levels a second empirically determined threshold is established. Peak values associated with a possible vortex must exceed this threshold before a decision is made to identify the vortex.

The vortex coordinates, x and y, are recorded on digital tape and used for the several plot options which are more fully described in paragraph 4.2.1.

4.1.2 Pulsed Mode Bistatic Forward Scatter Configuration

System operation in a pulsed-mode bistatic forward scatter configuration is similar to operation in the cw mode described above--with the following exceptions:

1) Only one transmitter assembly and one receiver assembly (12 microphone channels) need be activated, although two may be utilized for redundancy and/or to increase coverage.

2) Pulses of controlled carrier frequency, duration, and repetition period are generated.

3) Data processing requirements increase, reflecting the higher data rate resulting from adding time delay information.

The necessity for using data from two sets of receiving beams to measure the intersecting angle is alleviated if time delay information is available. Determination that a vortex-scattered path is longer by a particular amount than that of the line-of-sight pulse (excess path length) is used to specify the vortex position along an ellipse whose foci are the transmitter and receiver sites and whose axes are determined by the excess path length in a manner exactly analagous to the Pulsed Acoustic Vortex Sensing System*. Intersection of this ellipse with an elevation angle determined by a single 12-element receiver assembly uniquely defines the vortex position in terms of both altitude and horizontal displacement. Thus each transmitter-receiver pair can be used to make an independent estimate of both vortex locations. Since both pairs can be operated in this mode concurrently, two independent estimates of the same locations can be made and combined to form the final estimate.

All the pulsed mode configurations operate in a similar way through the process of determining a range and angle estimate for each vortex. Conversion of this range and angle estimate into vortex location is uniquely dependent on the actual geometry of the Doppler acoustic radar subsystem. The data specifying all element locations and elevation angles are keyboard entries by the operator.

The discussion of the pulsed mode operation continues in terms of the monostatic backscatter configuration. The terms range and elevation angle are unambiguous and most analogous to widely understood radar terminology for this mode and monostatic backscatter operation presents the greatest demand on the system processing capability.

4.1.3 Monostatic Pulsed Backscatter Configuration

In the cw mode, 36 samples of data must be processed for each receiver to locate the vortices in two intersecting elevation angles. In the pulsed mode, the vortex location is determined in range and elevation angle so that the three discriminant outputs for each beam of each receiver must be sampled at a rate which preserves the time delay

*Pulsed Acoustic Vortex Sensing System, Final Report, Volume II, Studies of Improved PAVSS Processing Techniques, Report Number FAA-RD-75-161, II, dated June 1977.

resolution allowed by the transmitted pulse length. The rate at which the data is sampled is controlled by the DMA scan period. It may be as short as 3 msec or a long as 2 seconds per scan. A short time constant for the individual filter detectors is automatically selected in this mode.

In this mode, one pulse is transmitted by each transmitter during each frame period. The time delay resolution with which the signal returns are sampled is controlled by the DMA scan period (msec/ scan of all selected channels). Since signal returns of interest are expected between a minimum and maximum delay from the initiation of the pulse, DMA scans are made only during that period. Initiation of the first DMA scan after pulse initiation is controlled by a keyboard selectable parameter and DMA scans continue at the DMA scan rate until a preselected DMA byte count (under keyboard control) is reached. The same process is repeated for each successive frame.

When the DMA transfer is complete, a section of the mini-computer core memory is filled with a matrix of MN values. M is three times the number of channels selected (i.e., 6, 12, or 24 beams) while N is the number of scans per frame period (i.e., the total number of range gates formed). This matrix is now searched in both angle and range to locate the up to two vortices expected. Again the principal search parameter used is the sum of intensity and spread for each range angle point. Skew is used as an aid in distinguishing the left from the right circulating vortex when only one vortex is present and as a check on relative position when two vortices are present. The average of the sum of intensity and spread in the longest range gate is used to set the thresholds for aircraft noise and false alarm rejection. In addition an exclusion zone is drawn around the strongest vortex. The exclusion zone prevents two estimates of vortex position being made on the same vortex from causing a failure to detect the second vortex.

Once the two estimates of vortex position are made in the range-angle space, each is checked against the false alarm threshold to determine whether it should be called a vortex. Having passed this test, its position in x - y space is calculated. This thresholding criteria is an empirically derived keyboard selectable parameter which automically operates on the current value of the average sum of intensity and spread in the longest range gate. If the estimate is accepted, the

vortex position is calculated using the Doppler acoustic radar subsystem site locations and elevation angles; and the calculated positions are used to determine the left and right vortex. This value is checked using skew when two vortices are present and is supplanted completely by skew when only one vortex is present.

4.2 DISPLAY FORMATS

Several display formats are available for CRT and hard copy data display. These are operator selectable for real time or playback viewing.

4.2.1 CRT Displays

The following CRT displays are available during real time or playback of DAVSS data:

1. Plot (P) (Figure 4-6). This consists of a single page with plots of height of each vortex versus time and horizontal position of both vortices versus time. The header data contains pertinent information for run identification. Included are array identification, run number, aircraft I.D., start-of-run time and mode. The time scales are in seconds and can be 60, 120 or 180 seconds, keyboard selectable.

2. Cross Plot (C) (Figure 4-7). This is a single plot of altitude versus horizontal distance. The same header data is used as described for the (P) Plot.

3. Diagnostic (D) Display (Figure 4-8). This presents an instantaneous picture of the three discriminates developed in the DAVSS from which vortex location is determined. The six columns are (from the left) spread, skew and intensity for receiver 1, and spread, skew and intensity for receiver 2. Symbols used show the level of signal present and in increasing order are (blank), : - + % # ■ Range increases toward the top of the page. Header data is the same as (C) and (P) Plots. The system does not make vortex location solutions when the (D) display is used.

4. Diagnostic Light Pen (DL) Display. This operator interactive display is the same as the (D) display except it allows the operator, by using the light pen, to track one vortex on the CRT screen from which vortex locations are formed by the system. (Can't be used in cw mode).

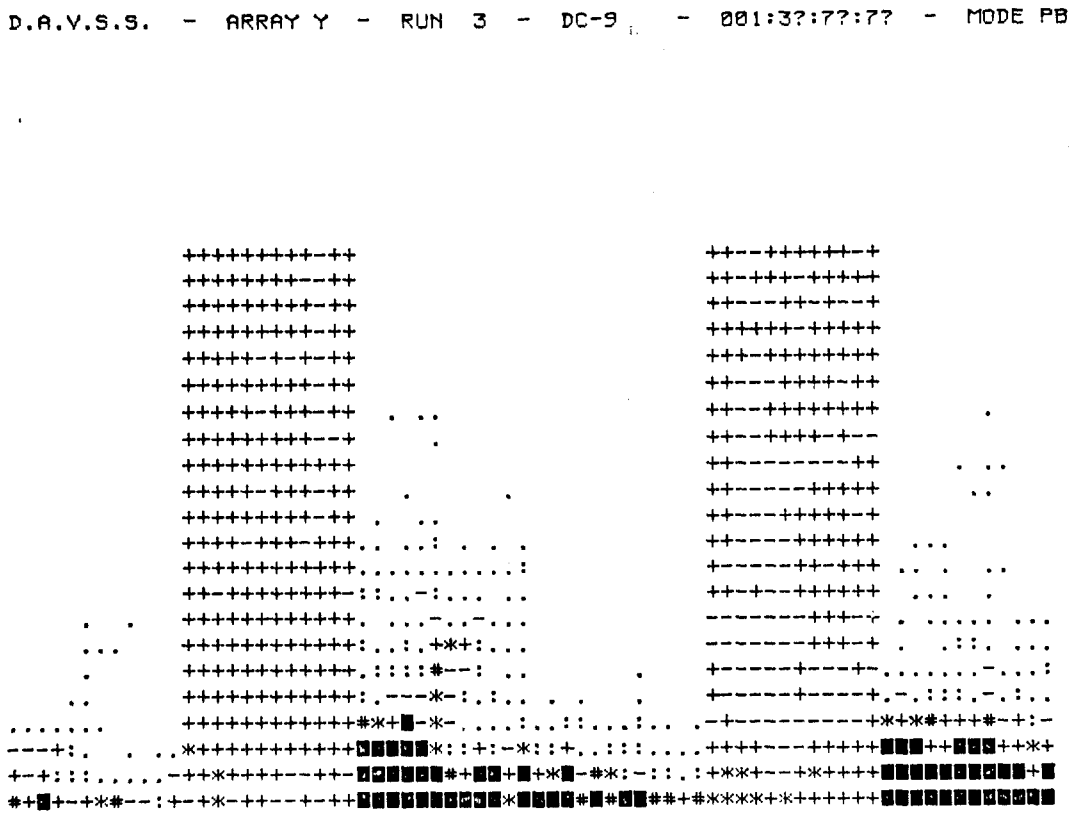


FIGURE 4-6. PLOT D

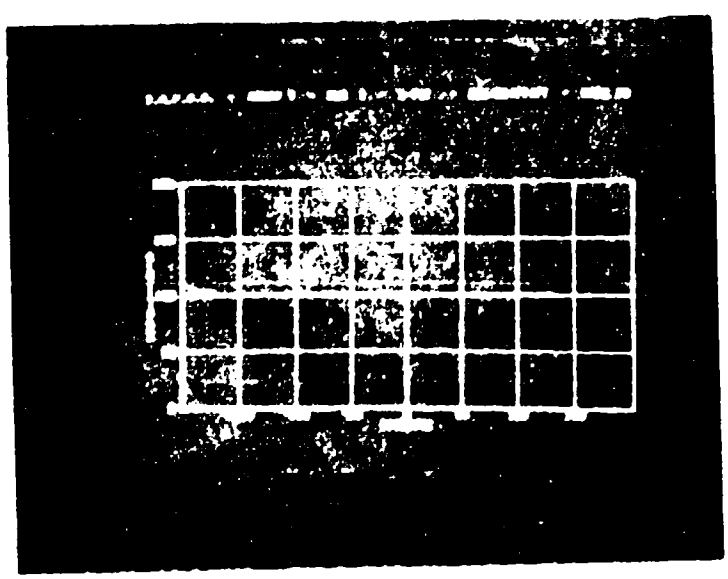


FIGURE 4-7. CROSS PLOT C

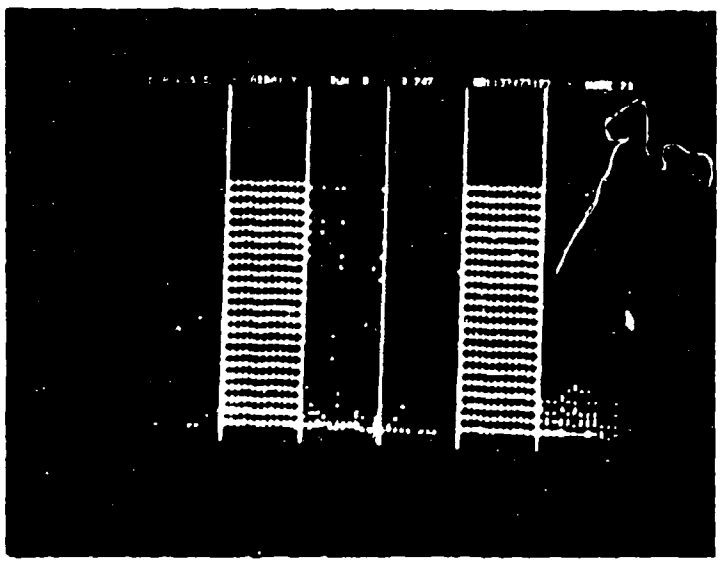


FIGURE 4-8. DIAGNOSTIC (D)

5. Raw Data (R_1 or R_2) display (Figure 4-9). Either the raw data outputs of receiver 1 or 2 of the array being operated can be displayed. This instantaneous display consists of twelve groupings of each of the six filter outputs for one receiver. The level of filter outputs are shown using the same symbols described for the (D) diagnostic display. Range increases toward the top of the page. The system does not determine vortex locations during this CRT display.

4.2.2 Hard Copy Displays

Several hard copy displays are available and are listed below:

1. Processing parameters (Figure 4-10). Upon command, the hard copy printer will print out the two pages of processing parameters currenly entered in the machine. During this printout all other functions of the system halt unitl the printout is completed.

2. Plot (P) printout (similar to CRT Figure 4-6). This printout is the same as the (P) Plot CRT display. Header data is the same as the CRT display except that the time scale is included and the start-of-run time is entered at the end of the plot.

3. Diagnostic printout (similar to CRT Figure 4-8). This printout when called for gives the discriminate data in the system at the time the printout was called for. During the printout the CRT diagnostic display freezes.

4. Raw data printout (similar to CRT Figure 4-9). Raw filter output data in the system is printed when the operator calls for it. The CRT display is frozen during the printouts.

4.3 OPERATING PROCEDURE

Operation of the DAVSS requires a specific procedure to be followed. Since the system is under computer control, input parameter limits and sequences of operation must be followed precisely or the system will halt or malfunction. The remainder of this section describes in a general manner the parameter limits and sequence of operations required for proper operation of the DAVSS. Step-by-step procedures are contained in the Operating Instructions (not part of this final report).

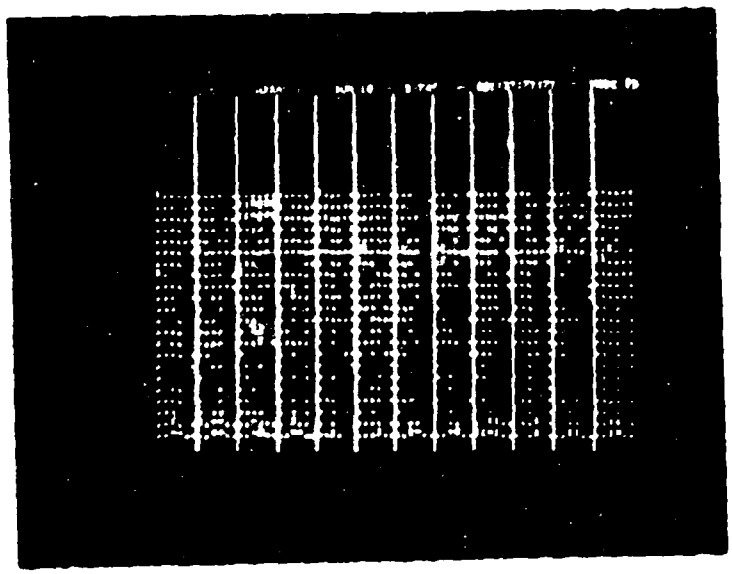


FIGURE 4-9. RAW DATA

D.A.V.S.S. PROCESSING PARAMETERS - PAGE 1

A = MODE (R.P) - PLOT TIME (1.2.3 MIN)	R	1
B = AUTO START - AUTO STOP (E.D)	D	D
C = DISPLAY MODE (GT-40) (VERS)	P	P
D = RANGE MIN - MAX (MSEC)	50	1000
E = RANGE GRANULARITY (MSEC)	29	
F = CENTER FILTER OFFSET (HZ)	100	100
G = MIDDLE FILTER OFFSET (HZ)	200	200
H = OUTER FILTER OFFSET (HZ)	300	300
I = CENTER FILTER WIDTH (-20 HZ)	3	3
J = MIDDLE FILTER WIDTH (-20 HZ)	3	3
K = OUTER FILTER WIDTH (-20 HZ)	3	3
L = NOTCH FILTER WIDTH (50 HZ)	1	1
M = CENTER DISC. GAIN (%)	50	50
N = MIDDLE DISC. GAIN (%)	75	75
O = OUTER DISC. GAIN (%)	100	100
P = DIAG. DISPLAY LIMITS - LOWER, UPPER (%)	10	90
Q = EXCLUSION ZONE - RANGE, BEAM		
R = THRESHOLDS - NOISE MULTIPLIER, A/C NOISE		
S = MIN. AND MAX. ALTITUDE (ELEMENT 1)		
T = MIN. AND MAX. ALTITUDE (ELEMENT 2)		

D.A.V.S.S. PROCESSING PARAMETERS - PAGE 2

A = ACTIVE ARRAY - PROCESSING MODE	Y	B
B = ACTIVE STATIONS - FRAME LENGTH (MSEC)	B	1000
C = AIRPORT CODE - TAPE NUMBER	A	1
D = WIND (FT/SEC) - REL HUM (%)	0.	50.
E = TEMP (DEG F) - DAY OF YEAR	70.	001:00:00:00
F = RAMP MIN GAIN (%)	0	10
G = RAMP MAX GAIN (%)	100	100
H = RAMP START (MSEC)	200	50
I = RAMP STOP (MSEC)	500	1000
J = PULSE [illegible] TIME (10 USEC)	2	2
K = PULSE [illegible] (MSEC)	15	15
L = [illegible]	3000	3000
M = [illegible]	-10.	10.
N = [illegible]	-25.	25.
O = [illegible]	30.	30.
P = [illegible]	-15.	15.
Q = [illegible]	-25.	25.
R = [illegible]	20.	20.

FIGURE 4-10. PROCESSING PARAMETERS

4.3.1 Program Loading

The operating program for the DAVSS is loaded from magnetic tape. A key switch on the GT-40 controls the power to the GT-40 processor, the CRT, the magnetic tape units and the hard copy printer/plotter. After the key is turned and all the above units are on, the DAVSS program tape is mounted on the TU-10 tape recorder. The tape is then threaded, drawn into the vacuum columns, and brought to the load point with the recorder off-line. Then the tape recorder is switched on-line and the bootsrap loader in the GT-40 is used to load the program. For this operation a specific sequence must be followed which uses the front panel switches of the GT-40 processor. The sequence is outlined step-by-step in the Operating Instructions. When the operating program is loaded, the first page of the Processing Parameters will appear on the CRT of the GT-40.

4.3.2 Processing Parameters

There are two pages of Processing Parameters by which the operator selects all the selectable parameters for DAVSS configuration control, mode selection, frequency, pulse shape, frame period, filter position and bandwidth, discriminant control, display selection, etc. These parameters are grouped on two pages such that page 2 contains all the parameters which effect the Doppler acoustic radar subsystem itself and which determine the character of data recorded on the analog tape. Page 1 contains the processing and display parameters which can be altered on playback and which affect the way the processing and display subsystems are functioning at the moment but don't affect the data being recorded or played back.

Figure 4-11 shows both pages of the Processing Parameters. The next steps are to enter the required data on the right-hand part of both pages. Figure 4-11 shows typical data only. Specific data required will depend on the specific siting configuration and experience with the optimal DAVSS performance in the various operating modes under varying operational conditions -- primarily noise and meteorological conditions. The parameter data entry is accomplished in a straight forward manner following the specified sequence. When a specific line is indentified for processing data entry from the keyboard, it is intensified on the CRT display. Data entries are shown on the CRT immediately and errors are signaled both audibly and by a blinking error message. When all processing parameters are entered to the operator's satisfaction, a permanent record may be generated, using the Versatec hard copy display.

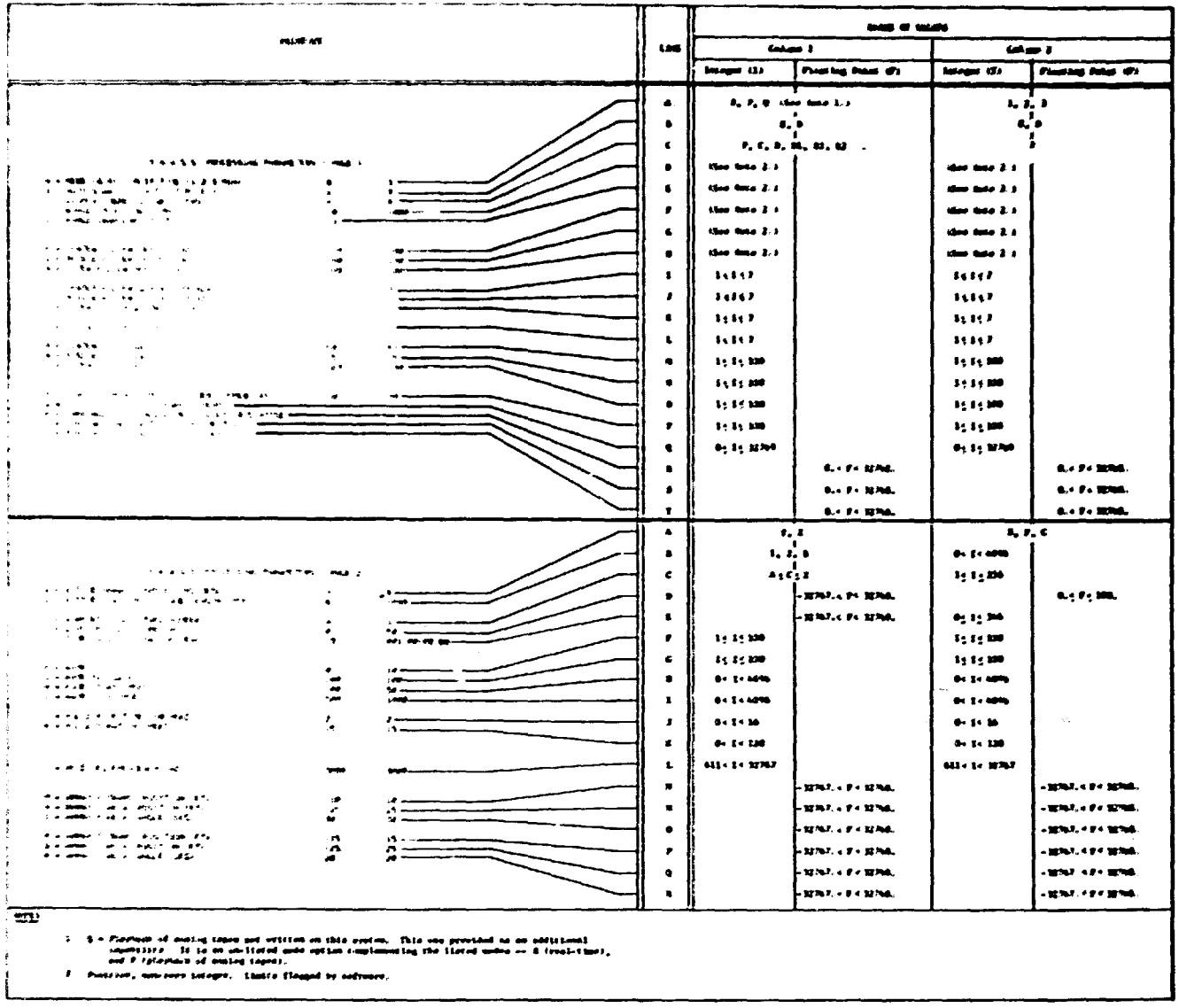


FIGURE 4-11. TYPICAL PROCESSING PARAMETER PRINTOUT (WITH LIMITS)

4.3.3 Data Recording

When the system operating program is loaded and the processing parameters entered, the system is ready for vortex detection and tracking. At this point the program tape is dismounted from the digital tape recorder, and data tapes are loaded on both the digital and analog tape recorders. In order to write digital data on the digital data tape, a WRITE ENABLE ring must be inserted on the rear of the fresh tape reel. After the analog tape is loaded on the VR3700B twenty-eight track recorder, in order to put the tape recorder under control of the DAVSS, the operator should make sure the PHASE Lock Selector (9) is on TACH, the RECORD Test Selector (10) is on NORM, and the TAPE Speed Selector (11) is on REMOTE.

4.3.4 Vortex Data Run

When the system is ready for vortex data collection, control of the system may be executed either directly from the GT-40 keyboard or from an external control box. In either case, the equivalent of a system ready signal causes the selected display to appear on the GT-40 with the leader showing the aircraft type, run number, mode of operation and a place for the start of run time. The system ready signal also causes the digital and analog tape recorder to begin recording.

When a Start of Run is initiated, the external time generator is read and the start of run time is deposited on the display and in the recorded data.

When the aircraft generated noise subsides the calculated vortex positon data is plotted on a frame update on the G T-40 and /or the hard copy display unit.

The run can be terminated either by a stop command, a new ready command, or automatically after 200 seconds.

For each succeeding run, the run number is automatically incremented and the aircraft identity is entered by way of the external control box.

APPENDIX A

DRAWINGS

NUMBER	TITLE
631830	DAVSS Receiver Ant. Assy.
631831	DAVSS Transmitter Ant. Assy.
631832	DAVSS Rec. & Trans. Sta. Tie Down
631833	DAVSS Cable Assy. Isolation Module to Ant.
631834	Wiring List -Cables Assy. (631833) Antennas
631835	CBA Sync Decode Module 1 Logic
631836	Schematic Diagram Sync Decode Mod. Logic
631837	CBA Sync Decode Module 2 Filter
631838	Schematic Diagram Sync Decode Mod. 2 Filter
631839	CBA DAV Primary Controller Bd. #1
631840	Schematic Diagram DAV Pri. Controller Bd. #1
631841	CBA DAVSS Controller Bd. #3
631842	Schematic Diagram DAVSS Controller Bd. #3
631843	CBA DAVSS Controller Bd. #2
631844	Schematic Diagram DAVSS Controller Bd. #2
631845	Component Board Assembly Dwg. Bds. 5&6
631846	Schematic Diagram Bds. 5&6
631847	CBA Configuration Control Module RCVR 1
631848	CBA Configuration Control Module RCVR 2
631849	Recorder Interface Schematic
631850	Interconnecting Cabling Diag. Assy.
631851	Schematic Diagram Analog Signal Processor
631852	CBA Configuration Control Module (XMTRS)
631853	CBA Line Driver & 6 Volt Regulator
631854	Schematic Diag. Envelope Modulator Board

NUMBER	TITLE
631855	Data Acquisition System Rack Layout
631856	Radar Controller Bd. 4
631857	Radar Controller Bd. 4 Schematics
631858	CBA Envelope Modulator Board Assy.
631859	Card Cage 3 Back Plane Wiring
631860	Card Cage 2 and 3 Back Plane Wiring
631861	CA-1 Cable Assembly Card File 3 to Card File 2
631862	CA-2 Cable Assembly Card File 3 to Card File 1
631863	CA-3 Cable Assembly Card File 1 to Analog Recorder
631864	CA-4 Cable Assembly Card File 2 to Analog Recorder
631865	CA-5 Cable Assembly Card File 3 to Analog Recorder and IRIG Input
631866	CA-6 Cable Assembly Card File 3 to Isolation Module and Message Code
631867	CA-7 IRIG Generator Cable to P28
631868	CA-8 DAVSS Power Distribution Wiring Diagram
631869	CA-9 Cable Assembly between Control Boards 5 and 6 and Signal Processor Boards
631870	CBA Analog Signal Processor Board

APPENDIX B

PARTS

DIGITAL EQUIPMENT CORPORATION (DEC) EQUIPMENT

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Graphic Display System	1	GT40-AA	DEC
2	Tape, Magnetic - ntrol and Transport	1	TM11-EA	DEC
3	Extended Arithmetic Unit	1	KE11-A	DEC
4	Bootstrap Loader	1	MR11-DB	DEC
5	Mounting Box Extension	1	BA11-ES	DEC
6	Power Supply	1	H720-E	DEC
7	Mounting Box, Peripheral	1	DD11-A	DEC
8	Memory System	1	ME11-LA	DEC
9	Cabinet	1	H960-CA	DEC

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Aluminum Box	1	CU-3003-A	Bud
2	Diode	6	1N3611	
3	Relays	4	HCM11D	P&B
4	Sockets, Relay (for HCM11D)	4		P&B
5	Board, Fiberglass, 4" x 2½"	1		
6	Resistor, 130 ohm, ½W	1	RC07GF131J	
7	Connector	1	PT02-12-10S	Bendix
8	Standoff	4	1-inch	
9	Grommet	1	½-inch ID	
10	Wire	A/R*	No. 24 AWG	
11	Connector (Reco nterface)			

* A/R = As Required.

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Tape Recorder, 28-channel, Intermediate Band, Magnetic, Reproduce System, Housed in a Cabinet and including the following-listed features: A. One track for voice logging B. Remote control configuration, with mating connector C. Tape Footage Counter	1	CPR4010/3700B	Bell & Howell

CARD CAGE NO. 1 ASSEMBLY

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Card Cage	1	706-9027-02-01-01	Cambion
2	Connector Block	1	201310-1	AMP
3	Connector Pin	A/R	66107-4	AMP
4	Connector Block	1	201356-1	AMP
5	Connector Block	1	200512-2	AMP
6	Connector Bracket	1		Avco
7	Connector Socket	1	66109-4	AMP
8	Wire (Wire-wrap)	A/R		Kynar
9	Wire	A/R	No. 20 AWG	

CARD CAGE NO. 2 ASSEMBLY

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Card Cage	1	706-9027-02-01-01	Cambion
2	Connector Block	1	20131-1	AMP
3	Connector Pin	A/R	66107-4	AMP
4	Connector Block	1	201356-1	AMP
5	Connector Block	1	200512-2	AMP
6	Connector Bracket	1		Avco
7	Connector Socket	1	66109-4	AMP
8	Wire (Wire-wrap)	A/R		Kynar
9	Wire	A/R	No. 20 AWG	

CARD CAGE NO. 3 ASSEMBLY

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Card Cage	1	706-9027-02-01-01	Cambion
2	Connector (Unibus)	1	H803	DEC
3	Connector Bracket (for H803)	1		Avco
4	Connector Bracket (for AMP Connector)	1		Avco
5	Card Separators	3	706-1021-02-00-00	Cambion
6	Cable, Unibus	1	BC11A-10	DEC
7	Wire (Wire-wrap)	A/R	No. 30 AWG	Kynar
8	Connector Block	1	201356-1	AMP
9	Connector Block	1	201532-4	AMP
10	Socket	A/R	66109-4	AMP
11	Connector Block	2	201310-1	AMP
12	Connector Pin	A/R	66107-4	AMP

CABLE ASSEMBLY (C/A) NO. 2

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Connector Block, P209P27	2	201311-1	AMP
2	Connector Socket	208	66109-4	AMP
3	Guide Pin	4		AMP
4	Jack Screw	2	201388-2	AMP
5	Wire	A/R	No. 26 AWG	
6	Clamp, Strain Relief	2	200730-1	AMP

CABLE ASSEMBLY (C/A) NO. 3

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Connector Block	1	201359-1	AMP
2	Connector Pin	24	66107-4	AMP
3	Cable, Coax	A/R	RG174/U	
4	Connector, BNC	12	KC-59-152	King

CABLE ASSEMBLY (C/A) NO. 4

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Connector Block	1	201359-1	AMP
2	Connector Pin	24	66107-4	AMP
3	Cable, Coax	A/R	RG174/U	
4	Connector, BNC	12	KC-59-152	King

CABLE ASSEMBLY (C/A) NO. 5

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Connector Block, P18	1	201692-4	AMP
2	Connector, J28	1	PT07P-20-39SW	Bendix
3	Connector, P30	1	MS3116-P12-10	
4	Connector, BNC	28	KC-59-159	King
5	Cable, Coax	A/R	RG174/U	
6	Wire	A/R	No. 22 AWG	
7	Connector Pin, P18	104	66107-4	AMP

CABLE ASSEMBLY (C/A) NO. 6

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Connector, J29	1	PT02CE-14-19S	Bendix
2	Connector, P16	1	AMP-104	AMP
3	Connector Block	1	201692-4	AMP
4	Connector Pin	A/R	66107-4	AMP
5	Wire	A/R	No. 24 AWG	

CABLE ASSEMBLY (C/A) NO. 7 (IRIG GENERATOR)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Connector	1	PT06P-20-39PW	Bendix
2	Connector	1	57-30500	Amphenol
3	Wire	168'	No. 20 AWG	
4	Cable, Coax	16'		
5	Connector, BNC	2	KC-59-152	King

POWER SUPPLY ASSEMBLY AND CABLE ASSEMBLY (C/A) NO. 8

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Power Supply, +15-Volt	1	PXS-D-15V	Power Mate
2	Power Supply, -15-Volt	1	PXS-D-15V	Power Mate
3	Power Supply, +24-Volt	1	PM-C-24V	Power Mate
4	Power Supply, +5-Volt	1	PM-E-5V	Power Mate
5	Connector	3	200346-2	AMP
6	Connector Pin	34	66109-4	AMP
7	Wire	A/R	No. 16 AWG, Teflon	
8	Wire	A/R	No. 14 AWG, Teflon	
9	Wire	A/R	No. 22 AWG, Teflon	
10	Resistor, 10 ohm, ½W	6	RC076F100J	
11	Terminal Strip	2	12-140	Cinch

CABLE ASSEMBLY (C/A) NO. 9

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Connector Wire/Assembly	4	16-006-116	Aries

ISOLATION MODULE

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Chassis	2	AC-427	Bud
2	Transformer	52	6T48HF	Allied
3	Lamp	104	WE-2	Chicago Miniature
4	Inductor	48	EA100	Triad
5	Resistor, 750 ohm, ½W	48	RC70-7515	TRW
6	Capacitor	48	WMF2P1	Cornell-Dubilier
7	Capacitor	48	WMF2P15	Cornell-Dubilier
8	Connector, Input	2	PT07A-24-61P	Bendix
9	Connector, Output	1	AMP104	AMP
10	Terminal Board	10	15233	Keystone
11	Wire	A/R	No. 24 AWG	

RADAR CONTROL BOARD NO. 4
(Page 1 of 2 pages)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	714-1115-01	Cambion
2	Socket, Wire-wrap, 16-Pin	105	703-3898-01-0316	Cambion
3	Socket, Wire-wrap, 28-Pin	1		Cambion
4	Header, Single (0.300), 16-Pin	9		Cambion
5	A/D Converter	1	ADC 540-8	Hybrid System, Inc.
6	Multiplexer	1	506A-5	Harris
7	Operational Amplifier	22	CA3100S	RCA
8	C/MOS 10-Bit Monolithic Multiplier D/A Converter	6	AD 7520JD	Analog Devices
9	Quad 2-Input Positive-NAND Gate	2	7400	
10	Quad 2-Input NAND Gate, Open Col.	8	7401	
11	Quad 2-Input Positive-NOR Gate	6	7402	
12	Hex Inverter	6	7404	
13	Dual 4-Input Positive-NAND Gate	3	7420	
14	Dual 4-Input NOR Gate, with Strobe	1	7425	
15	Quad 2-Input NAND Buffer	1	7437	
16	BCD to Decimal Converter	1	7442	
17	Dual D-Type Flip-Flop	1	7474	
18	Dual J-K Master-Slave Flip-Flop	1	74107	
19	Dual 4-to-1 Line Data Selector	2	74153	
20	Dual 2-to-1 Line Data Selector	12	74157	
21	Synchronous Counter	2	74161	
22	Monostable Multivibrator	1	74121	

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
23	Hex D-Type Flip-Flop	13	74174	
24	Quad D-Type Flip-Flop	9	74175	
25	Potentiometer, 10K	1	3099P-1-103	Bourns
26	Resistor, DIP, 10K	4	898-3-R10K	Beckman
27	Resistor, DIP, 1K	4	898-3-R1K	Beckman
28	Capacitor, 0.01 microF, 25-Volt	25		
29	Capacitor, 10 microF, 20-Volt	1		
30	Capacitor, 11 microF, 100-Volt	24	CK06BX104K	
31	Capacitor, 47 pF, 200-Volt	6	CK05BX470K	
32	Capacitor, 180 pF	24		
33	Capacitor, 0.001 microF, 200-Volt	1		
34	Capacitor, 17 pF	3		
35	Resistor, 1.2K, ¼W, 5%	1	RC07	
36	Diode	1	1N825	
37	Wire (Wire-wrap)	A/R	No. 30 AWG	Kynar
38	Adhesive	A/R	RTV 102	GE

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	714-1115-01	Cambion
2	Socket, Wire-wrap, 16-Pin	82	703-3898-01-0316	Cambion
3	Socket, Wire-wrap, 28-Pin	6		Cambion
4	Header, 16-Pin	1		Cambion
5	Capacitor, 0.01 microF, 25-Volt	16		
6	Capacitor, 0.05 microF	1	M39014/02-0266	
7	Capacitor, 1000 pF	2	M39014/01-0277	
8	Resistor, DIP, 10K	15	893-3-R10K	Beckman
9	Multiplexer		H-I-506A-5	
10	Quad 2-Input Positive-NAND Gate	1	7400	
11	Quad 2-Input Positive-NOR Gate	4	7402	
12	Hex Inverter	7	7404	
13	Hex Buffer/Driver	2	7407	
14	Dual 4-Input Positive-NAND Gate	1	7420	
15	BCD to Decimal Converter	1	7442	
16	4-Bit Magnitude Comparator	8	7485	
17	4-Bit Binary Counter	5	7493	
18	Dual J-K Master-Slave Flip-Flop	1	74107	
19	Monostable Multivibrator	1	74121	
20	Synchronous 4-Bit Counter	3	74163	
21	Hex D-Type Flip-Flop	6	74174	
22	Quad D-Type Flip-Flop	13	74175	
23	Quad Voltage Comparator	11	LM339	National Semiconductor
24	Capacitor, 10 microF, 20-Volt	1		
25	Wire (Wire-wrap)	A/R	No. 30 AWG	Kynar

RADAR CONTROLLER BOARD NO. 1
(Page 1 of 2 pages)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	714-1111-01	Cambion
2	Header, Double, 16-Pin	2	702-3730-01-03	Cambion
3	Header, Single, 16-Pin	4	702-3728-01-03	Cambion
4	Integrated Circuit, TTL	10	SP380	Signetics
5	Integrated Circuit, TTL	14	8881	TI
6	Integrated Circuit, TTL	8	SN7402N	TI
7	Integrated Circuit, TTL	13	SN7400N	TI
8	Integrated Circuit, TTL	15	SN7474N	TI
9	Integrated Circuit, TTL	12	SN7401N	TI
10	Integrated Circuit, TTL	8	SN74193N	TI
11	Integrated Circuit, TTL	9	SN7408N	TI
12	Integrated Circuit, TTL	2	SN7486N	TI
13	Integrated Circuit, TTL	4	SN7442N	TI
14	Integrated Circuit, TTL	2	SN74175N	TI
15	Integrated Circuit, TTL	2	SN7475N	TI
16	Integrated Circuit, TTL	1	SN74123N	TI
17	Integrated Circuit, TTL	1	SN74121N	TI
18	Integrated Circuit, TTL	10	SN7404N	TI
19	Integrated Circuit, TTL	2	SN7430N	TI
20	Resistor Pack, 1K	2	893-3-R, 1.0K	Beckman
21	Resistor Pack, 10K	1	898-3-R, 10K	Beckman
22	Resistor, 5.1K, 5%	1	RC07GF512J	M-S
23	Resistor, 470 ohm, 5%	11	RC07GF471J	M-S
24	Resistor, 10K, 5%	1	RC07GF103J	M-S

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
25	Resistor, 390 ohm, 5%	2	RC07GF391J	M-S
26	Resistor, 1K, 5%	4	RC07GF102J	M-S
27	Capacitor, 0.01 microF	4	HY520	Sprague
28	Capacitor, 330 pF	4	5GA-T33	Sprague
29	Capacitor, 50 pF	1	5GA-Q50	Sprague
30	Capacitor, 470 pF	5	5GA-T47	Sprague
31	Capacitor, 1800 pF	2	5GA-D18	Sprague
32	Capacitor, 680 pF	1	5GA-T68	Spragee
33	Wire (Wire-wrap)	A/R		Kynar

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	714-1111-01	Cambion
2	Header, Single, 16-Pin	1	702-3728-01-03	Cambion
3	Integrated Circuit, TTL	9	SN7400N	TI
4	Integrated Circuit, TTL	25	SN74175N	TI
5	Integrated Circuit, TTL	24	SN7485N	TI
6	Integrated Circuit, TTL	25	SN7493N	TI
7	Integrated Circuit, TTL	11	SN7474N	TI
8	Integrated Circuit	5	SN7404N	TI
9	Integrated Circuit, TTL	5	SN7402N	TI
10	Integrated Circuit, TTL	9	SN7490N	TI
11	Integrated Circuit, TTL	2	SN7408N	TI
12	Clock, 10 MHz	1	CO-238A	Vectron
13	Resistor, 1K, 5%	1	RC07GF102J	M-S
14	Wire (Wire-wrap)	A/R		Kynar

RADAR CONTROLLER BOARD NO. 3
(Page 1 of 2 pages)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	714-1111-01	Cambion
2	Header, Double, 15-Pin	3	702-3730-01-03	Cambion
3	Header, Single, 16-Pin	2	702-3728-01-03	Cambion
4	Integrated Circuit, TTL	7	SN7485N	TI
5	Integrated Circuit, TTL	1	SN7490N	TI
6	Integrated Circuit, TTL	12	SN7404N	TI
7	Integrated Circuit, TTL	1	SN7408N	TI
8	Integrated Circuit, TTL	7	SN7474N	TI
9	Integrated Circuit, TTL	6	SN7402N	TI
10	Integrated Circuit, TTL	13	SN7401N	TI
11	Integrated Circuit, TTL	9	SN7495N	TI
12	Integrated Circuit, TTL	7	SN7400N	TI
13	Integrated Circuit, TTL	10	SN74175N	TI
14	Integrated Circuit, TTL	1	SN7430N	TI
15	Integrated Circuit, TTL	3	SN74125N	TI
16	Integrated Circuit, TTL	4	SN7475N	TI
17	Integrated Circuit, TTL	6	SN7493N	TI
18	Integrated Circuit, TTL	2	SN7410N	TI
19	Integrated Circuit, TTL	1	SN74123N	TI
20	Relay Driver	2	SN7545N	TI
21	Resistor Pack	1	898-3-R1.0K	Beckman
22	Resistor, 1K, 5%	5	RC07GF102J	M-S
23	Resistor, 39K, 5%	2	RC07GF393J	M-S
24	Resistor, 20K, 5%	2	RC07GF203J	M-S

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
25	Capacitor, 0.01 microF	4	HY520	Sprague
26	Capacitor, 1 microF	3	CK06BX105K	M-S
27	Capacitor, 0.022 microF	1	CK06BX223K	M-S
28	Capacitor, 0.0022 microF	1	CK06BX222K	M-S
29	Capacitor, 470 pF	1	5GA-647	Sprague
30	Wire (Wire-wrap)	A/R		Kynar

FILTER BOARD (SYNC DECODE)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board , 56-Socket, 14-Pin	1	715-1106-01	Cambion
2	Header, Double, 14-Pin	8	702-3726-01-03	Cambion
3	Integrated Circuit, TTL	1	SN7401N	TI
4	Comparator	2	LM3111N	National
5	Operational Amplifier	8	747 DC	Fairchild
6	Capacitor, 0.001 microF, Poly.	6	E32B102FXW	Component Research Company
7	Capacitor, 0.2 microF, Poly.	2	E32B204FXW	Component Research Company
8	Capacitor, 0.01 microF, Poly	2	E32B103FXW	Component Research Company
9	Capacitor, 0.05 microF, Poly	2	E32B503FXW	Component Research Company
10	Resistor, 10K, 5%	26	RC07GF103J	
11	Resistor, 1K, 5%	4	RC07GF102J	
12	Resistor, 100K, 5%	3	RC07GF104J	
13	Resistor, 3K, 5%	2	RC07GF302J	
14	Resistor, 2K, 5%	2	RC07GF202J	
15	Resistor, 56K, 5%	1	RC07GF563J	
16	Resistor, 30K, 5%	1	RC07GF303J	
17	Resistor, 7.15K, 1%	2	RN55D7151F	
18	Resistor, 4.02K, 1%	2	RN55D4021F	
19	Resistor, 8.06K, 1%	2	RN55D8061F	
20	Resistor, 1.91K, 1%	3	RN55D1911F	
21	Resistor, 4.64K, 1%	1	RN55D4641F	
22	Resistor, 21.5K, 1%	1	RN55D2151F	
23	Resistor, 243K, 1%	1	RN55D2433F	
24	Wire (Wire-wrap)	A/R		Kynar

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, 56-Socket, 16-Pin	1		Cambion
2	Header, Single, 16-Pin	1		Cambion
3	Integrated Circuit, TTL	11	SN7485N	TI
4	Integrated Circuit, TTL	10	SN7474N	TI
5	Integrated Circuit, TTL	10	SN7493N	TI
6	Integrated Circuit, TTL	5	SN7495N	TI
7	Integrated Circuit, TTL	4	SN7400N	TI
8	Integrated Circuit, TTL	5	SN7404N	TI
9	Integrated Circuit, TTL	1	SN74123N	TI
10	Integrated Circuit, TTL	2	SN74221N	TI
11	Integrated Circuit, TTL	1	SN74121N	TI
12	Integrated Circuit, TTL	1	SN7427N	TI
13	Integrated Circuit, TTL	1	SN7490N	TI
14	Integrated Circuit, TTL	1	SN7408N	TI
15	Integrated Circuit, TTL	1	SN7402	TI
16	Resistor, 39K, 5%	2	RCO7GF393J	M-S
17	Resistor, 36K, 5%	2	RCO7GF363J	M-S
18	Resistor, 24K, 5%	1	RCO7GF243J	M-S
19	Resistor, 6.8K, 5%	1	RCO7GF682J	M-S
20	Capacitor, 333 picoF	1	5GA-T33	Sprague
21	Capacitor, 0.01 microF	4	HY520	Sprague
22	Capacitor, 0.1 microF	3	CKO6BX104K	Erie

CONFIGURATION CONTROL, RECEIVERS (2 EACH)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	715-1101-01	Cambion
2	Relay	7	KHP17D11	P&B
3	Relay Driver	1	SN75451N	TI
4	Diode	2	1N4003	
5	Capacitor, 10 microF, 20-Volt	1	CS13E106M	Sprague
6	Capacitor, 50 microF, 50-Volt	1	TVA1308	Sprague
7	Relay Socket and Retainer	7	9KH1	P&B
8	Wire (Wire-wrap)	A/R		Kynar
9	Socket, 16-Pin	1	703-3898-01-04-16	Cambion

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	715-1101-01	Cambion
2	Relay	5	KHP17D11	P&B
3	Relay Driver	2	SN75451N	TI
4	Diode	4	1N4003	
5	Capacitor, 10 microF, 20-Volt	1	CS13E106M	Sprague
6	Capacitor, 50 microF, 50-Volt	1	TVA1308	Sprague
7	Relay Socket and Retainer	7	9KH1	P&B
8	Wire (Wire-wrap)	A/R		Kynar
9	Socket, 16-Pin	1	703-3898-01-04-16	Cambion

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	715-1101-01	Cambion
2	Socket, 14-Pin	1	703-3897-01-04-16	Cambion
3	Socket, 36-Pin	2	703-4061-01-04-16	Cambion
4	Header, 36-Pin	2	702-3734-01-03-00	Cambion
5	Terminal	24	2043-2-05	Cambion
6	Heat Sink	2	6001B-15	Thermalloy
7	Heat Sink	1	6106	Thermalloy
8	Transistor	2	2N5191	
9	Transistor	2	2N4920	
10	Diode	6	1N914	
11	Operational Amplifier	1	747 DC	Fairchild
12	Operational Amplifier	2	LH0021CK	National
13	Resistor, 0.5 ohm, 2W, Wire-wound	4	RW80V	M-S
14	Resistor, 2K, 5%	6	RC07GF202J	M-S
15	Resistor, 2.7 ohm, 5%	2	RC07GF2R7J	M-S
16	Resistor, 10K, 1%	4	RN55D1002F	M-S
17	Resistor, 8.06K, 1%	2	RN55D8061F	M-S
18	Resistor, Selected, 1%	2	RN55D	M-S

ENVELOPE MODULATOR BOARD
(Page 1 of 2 pages)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	714-1115-01	Cambion
2	Socket, Wire-wrap, 14-Pin	23	703-3897-01-03-16	Cambion
3	Socket, Wire-Wrap, 16-Pin	70	703-3898-01-03-16	Cambion
4	Socket, Wire-wrap, 24-Pin	2		Cambion
5	Header, Single, 16-Pin	7		Cambion
6	Resistor, DIP, 6K	4	898-3-R6K	Beckman
7	Resistor, DIP, 4.7K	2	898-1-R4.7K	Beckman
8	Capacitor Network, DIP	2	936C222XOSR	Sprague
9	C/MOS 10-Bit Monolithic Multiplier D/A Converter	2	AD7520JD	Analog Devices
10	Sine Look-up Table	2	S8773	AMI
11	Quad 741 Operational Amplifier	5	RC4136D	Raytheon
12	Voltage Comparator	15	LM311N	
13	Quad 2-Input Positive-NAND Gate	1	7400	
14	Quad 2-Input Positive-NOR Gate	2	7402	
15	Hex Inverter	5	7404	
16	Hex Inverter (Low Power)	1	74L04	
17	Quad 2-Input Positive-AND Gate	1	7408	
18	Dual 4-Input Positive-NAND Gate	1	7420	
19	Quad 2-Input Positive-OR Gate	6	7432	
20	Dual D-Type Flip-Flop	1	7474	
21	4-Bit Binary Full Adder	4	7483	
22	Decade Counter	1	7490	
23	Dual Retriggerable Monostable Multivibrator	6	74123	

ENVELOPE MODULATOR BOARD
(Page 2 of 2 pages)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
24	Quad D-Type Flip-Flop	6	74175	
25	4-Bit Up/Down Counter	4	74192	
26	4-Bit Up/Down Counter	14	74193	
27	Quad $\overline{S}$ - $\overline{R}$ Latches	2	74179	
28	Capacitor, 339 pF, 10%	6		
29	Capacitor, 15 pF	4		
30	Capacitor, 0.01 microF, 25-Volt	22		
31	Capacitor, 51 pF	2	CM4ED510J-03	
32	Capacitor, 10 microF, 20-Volt	2	MS39003/01-2526	
33	Diode	1	1N4742	Motorola
34	Resistor, 120 ohm, ½W, 5%	1	RC20	
35	Resistor, 6.8K, ¼W, 5%	4	RC07	
36	Resistor, 510 ohm, ¼W, 5%	2	RC07	
37	Resistor, 10K, ¼W, 5%	2	RC07	
38	Resistor, 9.1K, ¼W, 5%	2	RC07	
39	Resistor, 18K, ¼W, 5%	2	RC07	
40	Resistor, 24K, ¼W, 5%	4	RC07	
41	Resistor, 30K, ¼W, 5%	2	RC07	
42	Resistor, 36K, ¼W, 5%	2	RC07	
43	Wire (Wire-wrap)	A/R	No. 30 AWG	Kynar
44	Adhesive	A/R	RTV102	GE

SIGNAL PROCESSOR BOARD
(Page 1 of 3 Pages)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
1	Circuit Board, Wire-wrap	1	714-1115-01	Cambion
2	Socket, 14-Pin, Wire-wrap	82	703-3897-01-03-16	Cambion
3	Socket, 16-Pin, Wire-wrap	8	703-3898-01-03-16	Cambion
4	Post, Wire-wrap to Solder	6	3866-01-04	Harvey/R&D
5	Socket, 36-Pin, Wire-wrap	6		Cambion
6	Header, Single (0.300), 16-Pin	2		Cambion
7	Header, Single (0.300), 14-Pin	16		Cambion
8	Header, 18-Pin (0.600), 36-Pin Socket	3		Cambion
9	Quad 741 Operational Amplifier	15	RC4136D	Raytheon
10	COS/MOS Quad Bilateral Switch	19	CD4016AF	RCA
11	C/MOS 10-Bit Monolithic Multiplier D/A Converter	1	AD7520J	Analog Devices
12	Regulator, 6-Volt	1	7S06393	Fairchild
13	Regulator, 12-Volt	1	LM340T-12	National Semiconductor
14	Transistor, Power, PNP, 4-Amp	2	MJE700	Motorola
15	Active Filter, Universal	6	881	Beckman
16	Diode Network, DIP, 14-Pin	3	899-60	Beckman
17	Capacitor Network, DIP, 16-Pin	1	936C222XO	Sprague
18	Capacitor Network, DIP, 16-Pin	1	936C103XO	Sprague
19	Capacitor Network, DIP, 14-Pin	2	934C104XO	Sprague
20	Resistor, DIP, 16-Pin, 3.3K	1	898-3-R3.3K	Beckman
21	Resistor, DIP, 16-Pin, 47K	1	898-3-R47K	Beckman
22	Resistor, DIP, 16-Pin, 68K	1	898-3-R68K	Beckman

SIGNAL PROCESSOR BOARD
(Page 2 of 3 pages)

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
23	Resistor, DIP, 14-Pin, 220 ohm	1	899-3-R220	Beckman
24	Resistor, DIP, 14-Pin, 1K	1	899-3-R1.0K	Beckman
25	Resistor, DIP, 14-Pin, 2.2K	1	899-3-R2.2K	Beckman
26	Resistor, DIP, 14-Pin, 6.8K	2	899-3-R6.8K	Beckman
27	Resistor, DIP, 14-Pin, 8.2K	1	899-3-R8.2K	Beckman
28	Resistor, DIP, 14-Pin, 10K	3	899-3-R10K	Beckman
29	Resistor, DIP, 14-Pin, 12K	3	899-3-R12K	Beckman
30	Resistor, DIP, 14-Pin, 16K	2	899-3-R16K	Beckman
31	Resistor, DIP, 14-Pin, 33K	7	899-3-R33K	Beckman
32	Resistor, DIP, 14-Pin, 47K	3	899-3-R47K	Beckman
33	Resistor, DIP, 14-Pin, 68K	2	899-3-R68K	Beckman
34	Resistor, DIP, 14-Pin, 100K	2	899-3-R100K	Beckman
35	Potentiometer, DIP, 10K	2	3099P-1-103	Bourns
36	Fixed Resistor, Selectable, 16K	4	4002)-1-163	Bourns
37	Fixed Resistor, Selectable, 8K	2	4002P-1-802	Bourns
38	Diode, Germanium	6	1N198	
39	Diode, Zener, 8.2-Volt	1	1N4738	Motorola
40	Capacitor, 150 microF, 15-Volt, DC	4	M39003/01-2277	
41	Capacitor, 470 pF	4		
42	Capacitor, 3.3 microF, 15-Volt, DC, 10%	6	150D335X9015A2	
43	Capacitor, 40 microF, 10-Volt, DC, 20%	2	150C406X9010B0	
44	Capacitor, 0.1 microF, 100-Volt, 2%	12		Callins
45	Resistor, 360K, ½W, 5%	10	RC07	

ITEM NO.	NOMENCLATURE AND DESCRIPTION	QUANTITY	PART NUMBER	MANUFACTURER
46	Resistor, 180K, ¼W, 5%	4	RC07	
47	Resistor, 330 ohm, ¼W, 5%	1	RC07	
48	Resistor, 56 ohm, ¼W, 5%	1	RC07	
49	Resistor, 33 ohm, ¼W, 5%	4	RC07	
50	Resistor (Selected at test)	6	RC07	
51	Heat Sink, for DIP	1		Astrodyne
52	Thermal Bond	A/R	Thermal	Astrodyne
53	Insulator, for Voltage Regulator	1	43-77-7	Thermalloy
54	Heat Sink, for Regulator and Transistor	1		Avco
55	Screw, Nylon, 4/40	2	2520	H.H. Smith
56	Screw, Nylon, 6/32	2	2526	H.H. Smith
57	Nut, Nylon	2	2555	H.H. Smith
58	Wire (Wire-wrap)	A/R		Kynar
59	Service, Wire-wrap		WS719-φ648	Cambion
60	Socket, Wire-wrap, 16-Pin (on board no's. 11, 12, 23, and 24 only)	2	703-3898-01-03-16	Cambion

APPENDIX C

RESULTS OF EARLY FIELD TESTS

Early field tests were conducted at Logan International Airport in July and August 1974. In these tests, one transmitting antenna assembly and one receiving antenna assembly, along with the necessary signal exciter, processing, and recording subsystems were installed at the ILS transmitter site for runway 22L. The antennas were configured for quasi-monostatic pulsed backscatter operation with the geometry shown in Figure C-1.

During these tests, evaluations of the performance of several of the critical analog subsystems were conducted. These included the envelope modulator, the receiver subsystem, the analog signal processor, and the data compression, multiplexing and A/D conversion circuits.

The purpose of the pulse shaping network in the envelope modulator was to reduce the spectral broadening of the transmitted signals. Various combinations of pulse delay and dwell time were tested by spectrum analyzing the received backscattered signals using a Saicor analog-digital hybrid spectrum analyzer. The network proved to be highly effective in limiting the bandwidth to less than the resolution capability of the analyzer.

The entire receiving antenna subsystem was evaluated for its ability to receive and detect the signals in the field of view while reducing the response to ambient noise. The side lobe reduction is manifest by measurement of the ambient noise level which was less than 50mv and the receiver sensitivity is manifest by measurement of the clutter amplitude versus range. The direct signal level was greater than 5V thus giving better than 40 db SNR. The gain ramp is utilized on playback to apply increasing gain with increased range.

The analog signal processor was evaluated for its capability to provide representative spectral samples of the complex signal spectral shape as compared to the output of a spectrum analyzer. Data from vortex detections was processed through the spectrum analyzer and displayed on a facsimilie recorder and compared with the same data processed through the analog signal processor (ASP) also displayed on the fac-

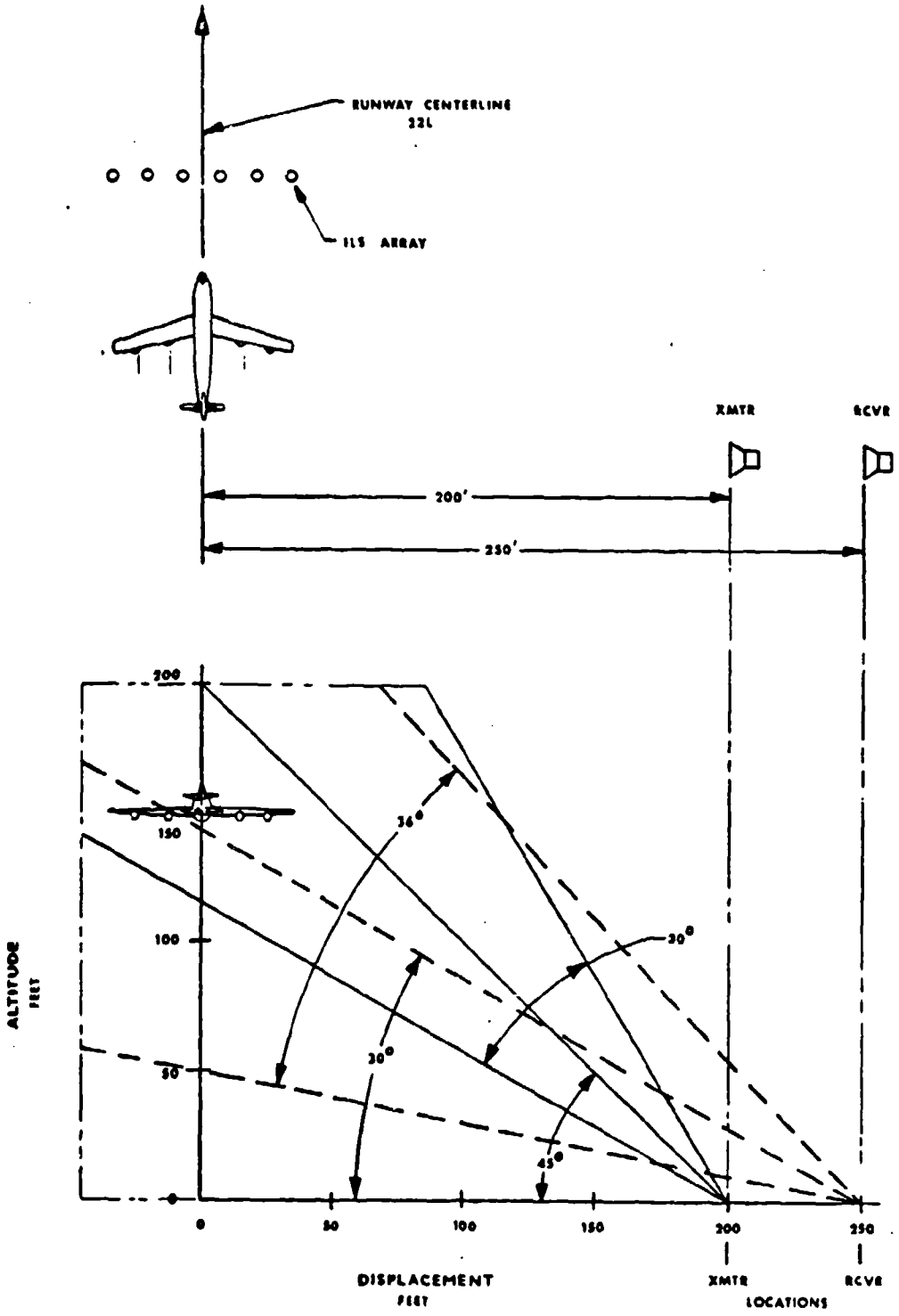


FIGURE C-1. RUNWAY/ARRAY GEOMETRY

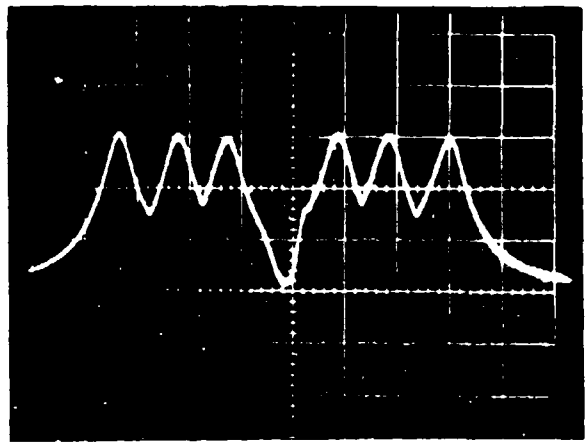
similie recorder. Although the ASP data was obviously more quantized because of the use of six discrete filters, all the recognizable and characteristic features of the vortex detection data were preserved.

Tests were conducted in which a sweeping frequency was inserted in the inputs to the ASP boards and the outputs of the detected filters summed and displayed on an oscilloscope. The resulting display in Figure C-2 shows the frequency response of a typical set of comb filters. These were adjusted to be equal within 1db. Operation of the data compression, multiplexing, and A/D conversion circuitry was evaluated along with the mini-computer and display routines by displaying first the raw filter data output and then the discriminant output for the sweeping frequency input and noting the display change during the sweep.

The prime goal of the Logan Airport early field tests was to collect quasi-monostatic backscatter data on tape for vortex detection and tracking capability demonstration. Data was recorded during several days of landing operations on runway 22L. However, due to coverage limitations caused by siting constraints (see Figure C-1) and the use of a single transmitting and receiving antenna assembly, suitable data was recorded only when the cross winds were low or when they blew the vortices through the field of view. Approximately forty aircraft data runs were recorded under these conditions. Several of these were utilized extensively in order to tailor the choice of the selectable processing parameters to optimize the detection and tracking results on this limited sample.

Figure C-3 shows the Versatec plot output from the detection and tracking of one run in which both vortices passed through the field of view. The aircraft type was an Electra. The transmitted frequency was 3,333 Hz, the pulse length 20 ms and the repetition period 700 ms. Valid tracking data begins about 12 seconds after aircraft passage and continues for another 16 seconds or so for the starboard vortex.

Tracking capability in the quasi-monostatic backscatter mode was clearly demonstrated in this test in which the Logan Airport recorded data were run through the DAVSS in the Q-back mode and the detection and tracking was done automatically in playback time; i.e., no lag from playback to display. The early field tests were successful in validating the performance of the analog subsystems evaluated and in providing a data base, albeit limited, on which to verify and modify the system processing and search routines before deployment of the DAVSS at J. F. Kennedy Airport.



Note:

Filters set at displacements of 100, 200 and 300 Hz;
20-Hz bandwidth.

FIGURE C-2. FREQUENCY RESPONSE OF THE SIX COMB FILTERS OF RECEIVER 1, BEAM 12

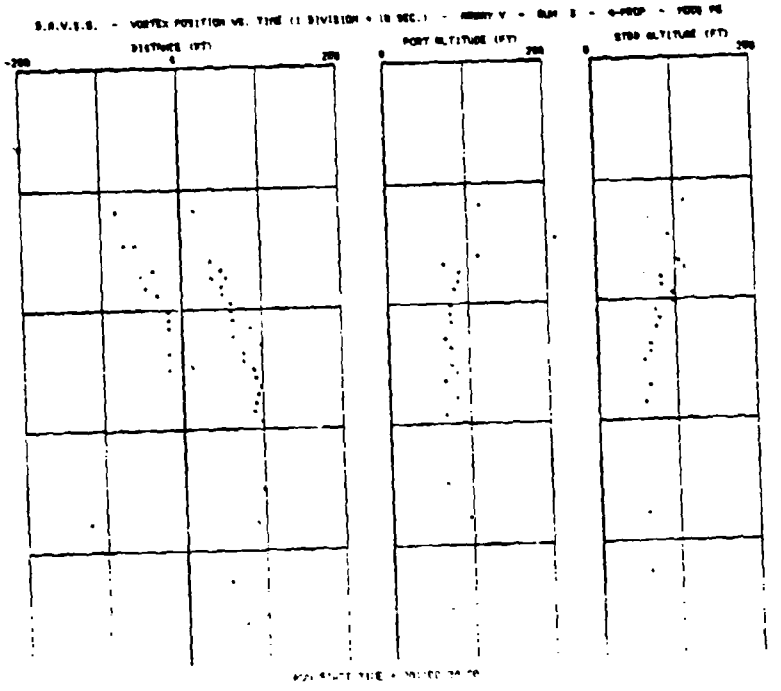


FIGURE C-3. PLOT OF ELECTRO-VORTEX DETECTION

APPENDIX D

REPORT OF INVENTIONS

This program resulted in the design, fabrication, and checkout of a real-time, minicomputer-controlled aircraft trailing vortex data collecting and display system. The effort was performed by Avco S/D under contract to the U.S. Department of Transportation. The hardware and software included many state-of-the-art applications of existing technology. These are described below.

The feasibility of acquiring aircraft trailing vortex position and strength histories using Doppler acoustic techniques was shown by the U.S. Department of Transportation, Transportation Systems Center. The results were obtained by in-the-field measurements using laboratory-type hardware. The recorded results were subsequently reduced using manual data reading and computer program support.

Avco S/D designed, fabricated, and checked out a real-time data acquisition, processing, and display system based on the DOT/TSC approach. This system was installed and operated successfully at John F. Kennedy International . irport, New York, as described in "Installation and Test of Doppler Acoustic Sensor", Report Number FAA-RD-76-223, dated October 1977.

The outstanding features of the hardware design were clever applications of current technology. The system was required to generate, transmit, receive, and analyze (in both frequency and intensity) acoustic signals. A minicomputer was used to control and sequence the operating system, as well as to perform numerical calculations and to format and display data.

Control

Control of acoustic transmit pulses or continuous waves (CW) was implemented by a digitally controlled, variable count-down generator. The generator output was amplitude-modulated using a multiplying digital-to-

analog converter driven by the CW signal and multiplied by the output of a sine/cosine read-only-memory as addressed by the computer.

System control flexibility was designed in by providing for operator keyboard input to an operating parameter table stored in the computer and displayed on the CRT terminal. After system experience was gained, a standard set of input parameters was provided at initial system turn-on so that the operator did not need to provide any input other than run start/stop functions.

Digital frequency control was used to control the frequency analyzer. Filters were arrayed symmetrically about a computer-selected center frequency. This was accomplished by translating the received signals down in frequency to a fixed center frequency to maintain a low frequency times Q (f x Q) product for filter stability. The separation of the filters from this center frequency was digitally controlled by the computer using CMOS switches which changed resistors in the filter circuits.

Processing

To conserve hardware and computer time, the received data was multiplexed. Weighing circuits sampled the filter outputs to develop discriminants representing input data for the processing algorithm. Initially, frequency spread, frequency skew, and intensity were used to determine the location of the center of the vortex. Later, a normalized and spatially averaged approach was implemented in the field. This yielded much better results.

Software

System software consists of a combination of several program modules. The operating features described in the body of this report were implemented using standard software design approaches.

It is the opinion of the author that although this system is very complex, and although the combination of hardware and software technology is clever, there are no patentable features since the techniques are individually well known.

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